SIEMENS

Data Book 1980/81

Digital ICs

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SIEMENS AKTIENGESELLSCHAFT

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Memory devices

Summary of preferred ICs made by AMD, Advanced Micro Devices Inc., available from SCS

Analog ICs

Type	Ordering code	Description
Operational amplifiers		
LF 398 H	Q 67000-A 1400-F 116	Sample and hold amplifier
LM 301 AH	Q 67000-A 118-F 116	General purpose op amp
LM 308 AN	Q 67000-A 1192-F 116	Instrumentation op amp
LM 310 N	Q 67000-A 1401-F 116	High speed voltage follower
LM 318 N	Q 67000-A 1179-F 116	High speed op amp
LM 319 N	Q 67000-A 1159-F 116	Dual comparator
AM 1500 DC	Q 67000-A 1769-F 116	Dual comparator
AM 1501 DC	Q 67000-A 1768-F 116	Dual op amp
Field effect operational amplifiers		
LF 355 H	Q 67000-A 1261-F 116	FET input op amp
LF 356 H	Q 67000-A 1502-F 116	FET input op amp
LF 357 H	Q 67000-A 1398-F 116	FET input op amp
D/A converters		
DAC 08 CN	Q 67000-U38-F 116	8-bit D/A converter
AM 6080 PC	Q 67000-A 1766-F 116	8-bit D/A converter, 20 pins
AM 6081 PC	Q 67000-A 1767-F 116	8-bit D/A converter, 24 pins
Interface devices		
N 8T 26 AB	Q 67000-H 2010-F 116	Quad BUS transceiver
N 8T 28 N	Q 67000-H 2009-F 116	Quad BUS transceiver
DP 8303 N	Q 67000-H 2008-F 116	Octal transceiver
DP 8304 BN	Q 67000-H 2006-F 116	Bidirectional transceiver

Summary of Types

ICs of the low power Schottky series (LS)[1])

Type	Ordering code	Description
AM 25 LS...		
240 PC	Q 67000-H 1453-F 116	Inverting octal BUF/driver 3-st out
241 PC	Q 67000-H 1454-F 116	Non-inverting octal BUF/driver 3-st out
242 PC	Q 67000-H 1593-F 116	Inverting quad transceiver 3-st out
243 PC	Q 67000-H 1584-F 116	Non-inverting quad transceiver 3-st out
244 PC	Q 67000-H 1555-F 116	Non-inverting octal BUF/driver 3-st out
273 PC	Q 67000-J 803-F 116	Octal D register: common clear
273 BPC	Q 67000-H 2026-F 116	Octal D register: clear
299 PC	Q 67000-J 1028-F 116	8 bit universal shift register
373 PC	Q 67000-Y 640-F 116	Octal transparent latch
374 PC	Q 67000-J 942-F 116	Octal D register: 3-st out
377 PC	Q 67000-J 943-F 116	Octal D register: common enable
377 BPC	Q 67000-H 2027-F 116	Octal D register: enable
381 PC	Q 67000-H 1641-F 116	4 bit function generator
2513 PC	Q 67000-H 1644-F 116	Priority interrupt encoder, 3-st out
2516 DC	Q 67000-Y 641-F 116	8 × 8 multiplier/accumulator
2517 PC	Q 67000-H 1645-F 116	ALU/function generator: carry look-ahead and overflow detection
2518 PC	Q 67000-J 1036-F 116	Quad D register, standard and 3-st out
2519 PC	Q 67000-J 1037-F 116	Quad D register: dual 3-st out
2520 PC	Q 67000-J 1038-F 116	Octal D register
2521 PC	Q 67000-H 1046-F 116	8 bit equal to comparator
2535 PC	Q 67000-Y 470-F 116	8 bit multiplexer
2536 PC	Q 67000-Y 471-F 116	1 of 8 decoder, control storage

[1]) Corresponds to the Texas Types SN 74 LS... N. The components are stamped with both type designations.

ICs of the low power Schottky series (LS)[1]

Type	Ordering code	Description
AM 25 LS...		
2537 PC[1]	Q 67000-H 1647-F 116	1 of 10 decoder, 3-st out polarity control
2538 PC[1]	Q 67000-H 1648-F 116	1 of 8 decoder, 3-st out polarity control
2539 PC[1]	Q 67000-H 1649-F 116	Dual 1 of 4 decoder, 3-st out polarity control
2568 PC[1]	Q 67000-J 1039-F 116	Synchronous BCD decade up-down counter, 3-st out
2569 PC[1]	Q 67000-J 1040-F 116	Synchronous 4 bit binary up-down counter, 3-st out
AM 25 LS...		
07 PC	Q 67000-J 1032-F 116	6 bit register: common enable
08 PC	Q 67000-J 1058-F 116	4 bit register: common enable
09 PC	Q 67000-J 1033-F 116	4 bit register: multiplexed inputs
14 PC	Q 67000-Y 469-F 116	8 bit serial parallel two's complement multiplier
15 PC	Q 67000-H 1643-F 116	4 bit serial parallel adder subtractor
22 PC	Q 67000-J1034-F 116	8 bit serial parallel register
23 PC	Q 67000-J 1035-F 116	8 bit universal shift register synchronous clear
AM 26 LS...		
31 PC	Q 67000-L 262-F 116	Quad differential line driver RS-422
32 PC	Q 67000-L 263-F 116	Quad differential line receiver RS-422/ RS-423
33 PC	Q 67000-L 264-F 116	Quad differential line receiver
MC 3448 AP	Q 67000-H 2007-F 116	Quad bidirectional transceiver
AM 27 LS...		
00 PC	Q 67000-Q 181-F 116	256 bit RAM, 3-st out
01 PC	Q 67000-Q 182-F 116	256 bit RAM – open collector
02 PC	Q 67000-Q 183-F 116	64 bit RAM – open collector
03 PC	Q 67000-Q 184-F 116	64 bit RAM – 3-st out

[1]) Corresponds to the Texas Types SN 74 LS... N. The components are stamped with both type designations.

ICs of the Schottky series (S)

Type	Ordering code	Description
AM 25 S...		
05 PC	Q 67000-H 2011-F 116	4 × 2 complement multiplier
07 PC	Q 67000-H 2012-F 116	6 bit register
08 PC	Q 67000-H 2013-F 116	4 bit register
09 PC	Q 67000-H 2014-F 116	4 bit register multiplexed inputs
10 PC	Q 67000-H 2015-F 116	4 bit shifter, 3-st out
18 PC	Q 67000-H 2016-F 116	Quad D register, 3-st out
557 DC	Q 67000-H 2017-F 116	8 × 8 bit combinatorial multiplier incl. register
558 DC	Q 67000-H 2018-F 116	8 × 8 bit combinatorial multiplier
SN 74 S...		
160 N	Q 67000-J 1030-F 116	BCD decade counter: asynchronous clear
161 N	Q 67000-J 1031-F 116	4 bit binary counter: asynchronous clear
240 N	Q 67000-H 1328-F 116	Inverting octal BUF/driver, 3-st out
241 N	Q 67000-H 1329-F 116	Non-inverting octal BUF/driver, 3-st out
242 N	Q 67000-H 2019-F 116	Inverting quad transceiver, 3-st out
243 N	Q 67000-H 2020-F 116	Non-inverting quad transceiver, 3-st out
244 N	Q 67000-H 1642-F 116	Non-inverting octal BUF/driver 3-st out
350 N	Q 67000-H 2021-F 116	4 bit shifter: 3-st out
373 N	Q 67000-J 923-F 116	Octal transparent latch, clear 3-st out
374 N	Q 67000-J 808-F 116	Octal register clock, 3-st out
378 N	Q 67000-H 2022-F 116	6 bit register: common enable
379 N	Q 67000-H 2023-F 116	4 bit register: common enable
388 N	Q 67000-H 2024-F 116	Quad D register: standard and 3-st out
399 N	Q 67000-H 2025-F 116	4 bit register: multiplexed inputs
AM 26 S...		
02 PC	Q 67000-K 104-F 116	Dual one-shot

Microcomputers System AM 2900

Microprocessors which can be cascaded, comprising 4 bit word length (so-called 4 bit slices), high operating speed and low power consumption.

Microprocessor kit AM 2900

Type	Ordering code	Description
AM 2900 K 1	Q 67201-C 8-F 116	Learning and evaluation kit
Microprocessor devices AM 2900		
AM 2901 BDC	Q 67020-C 16-F 116	Improved speed 4 bit
AM 2901 BPC	Q 67020-C 17-F 116	microprocessor slice
AM 2902 PC	Q 67020-P 9-F 116	High-speed look-ahead carry gen.
AM 2903 DC	Q 67020-C 11-F 116	Advanced 4bit bipolar µP slice
AM 2904 DC	Q 67020-Y 82-F 116	Status and shift-control-unit
AM 2905 PC	Q 67020-P 10-F 116	Quad 2-input oc bus transceiver with 3-state receiver
AM 2906 PC	Q 67020-P 11-F 116	Quad 2-input oc bus transceiver with parity
AM 2907 PC	Q 67020-P 12-F 116	Quad bus transceiver with interface logic
AM 2908 DC	Q 67020-Y 83-F 116	4-bus transceiver with interface logic
AM 2909 PC	Q 67020-C 9-F 116	Microprogram sequencer
AM 2910 DC	Q 67020-C 12-F 116	Microprogram controller
AM 2911 PC	Q 67020-C 10-F 116	Microprogram sequencer
AM 2913 PC	Q 67020-P 20-F 116	Priority interrupt expander
AM 2914 DC	Q 67020-P 13-F 116	Vectored priority interrupt controller
AM 2915 APC	Q 67020-P 14-F 116	Quad 3-state bus transceiver with interface logic
AM 2916 APC	Q 67020-P 15-F 116	Quad 3-state bus transceiver with interface logic
AM 2917 APC	Q 67020-P 16-F 116	Quad 3-state bus transceiver with interface logic
AM 2918 PC	Q 67020-P 17-F 116	Quad register with standard and 3-state outputs
AM 29 LS 18 PC	Q 67020-P 18-F 116	Quad register with standard and 3-state outputs
AM 2919 PC	Q 67020-P 19-F 116	Quad register with dual 3-state outputs
AM 2920 PC	Q 67020-P 20-F 116	Octal flip-flop with clear, clock enable and 3 state control

Summary of Types

System AM 2900

Type	Ordering code	Description
AM 2921 PC	Q 67020-Y 46-F 116	1 of 8-decoder with 3-state outputs and polarity control
AM 2922 PC	Q 67020-Y 47-F 116	8-input multiplexer w. control reg.
AM 2942 DC	Q 67020-Y 63-F 116	Programmable timer/counter, DMA address generator
AM 2950 DC	Q 67020-Y 85-F 116	8bit bidirectional I/O ports
AM 29701 PC	Q 67020-Q 4-F 116	Non-inverting schottky 64 bit RAM
AM 29803 ADC	Q 67020-Y 48-F 116	16-way branch control-unit
AM 29811 ADC	Q 67020-Y 50-F 116	Next address control-unit

1. Type nomenclature for ICs
(proelectron code)

The type nomenclature for digital ICs is constructed as follows:

FZ	H	10	5	A
Series code	Function	Number	Temperature	Variant

The series code for digital circuits is varied: FL, FZ, GD, ...
For individual digital ICs, the series code SA, SB, ... is used, the code UA, UB, ... being used for types which process analog and digital signals.

The function code has the following meaning:

H Logic gate
J Sequence control logic (static)
K Monostable circuit
L Level converter
N Sequence controlled logic (dynamic)
Q Memory matrix
R Read only memory
S Read amplifier with digital output
Y Various circuits not included in H to S

The serial number is sequential in the range 10 ... 99.

The variant specifies that this circuit differs electrically or mechanically from the original.

The temperature code specifies the operating temperature range as follows:

Old code	Temperature range	New code
0	Not defined	
1	0 to 70°C	B
2	−55 to 125°C	C
3	−10 to 85°C	–
4	+15 to 55°C	–
5	−25 to 85°C	E
6	−40 to 85°C	F
–	−25 to 70°C	D

In 1973, the type code for ICs was changed. The new code differs from the previously used code:
1. by specification of the temperature range with a letter in the series code
2. by the use of an existing type number as the serial number.

Example:

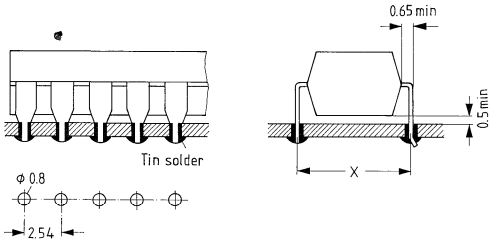
GX	B	10000	A
Series code	Temperature	Number	Variant

Siemens nomenclature
Standard devices which are intended for a restricted range of applications are designated with S and a three-digit number.

2. Mounting instructions

2.1 Plastic plug-in package

Plastic packages are soldered to the side of the printed circuit board away from the case. The pins are bent downwards at an angle of 90° and inserted into holes at equal distances of 2.54 mm and a diameter of 0.7 to 0.9 mm. The dimension X is shown in the corresponding package outline drawing.
The bottom of the package does not touch the printed circuit board after insertion, because the pins have shoulders just below the package (see figure).
After inserting the package into the printed circuit board, two or more pins should be bent at an angle of approximately 30° to the printed circuit board so that the package does not need to be held down while soldering. The maximum permissible soldering temperature for iron soldering is 265° C (max. 10 s) and for dip soldering 240° C (max. 4 s).



2.2 Flat package

a) Soldering on the side away from the package
The pins are bent downwards at an angle of 90° and inserted into holes with a diameter of 0.6 to 0.8 mm in the printed circuit board. The dimension X is shown in the corresponding package outline drawing. The pins may be bent at right angles at a distance of 0.8 mm or more from the case (figure 1).
The pins can be soldered by dip soldering or by iron soldering. At a solder bath temperature of 250° C, the maximum soldering time is 5 s; at 300° C, it is 2 s. After inserting the package in the printed circuit board, it is advisable to bend two (or all) pins at an angle of approx. 30° to the printed circuit board (figure 1), so that the package does not need to be held down during soldering. Excess lengths of connection pins should be removed before soldering.

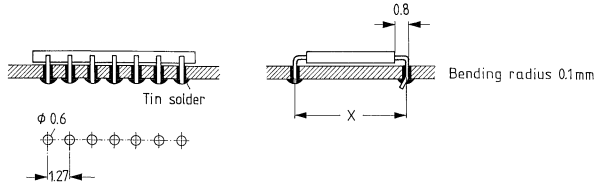


Figure 1

Dimensions in mm

b) When soldering on the upper side of the printed circuit board (figure 2), it is not necessary to drill holes in the board. The package pins can be connected to the printed wiring either by iron soldering or by welding.
The maximum soldering times, at a soldering distance $l \geqq 1.5$ mm, are $t_{max} = 15$ s for an iron temperature of 250° C, $t_{max} = 12$ s for 300° C, and $t_{max} = 7$ s for 350° C.

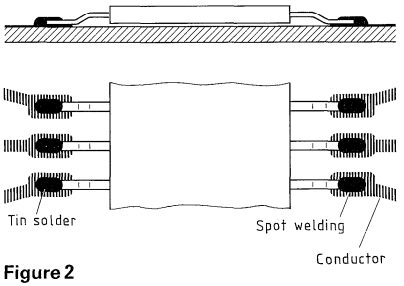


Figure 2

2.3 Package 5H8 DIN 41873 and similar packages with 8, 10, and 12 pins

The position of the case is arbitrary. The pins may be bent sideways at a minimum distance of 1.5 mm from the case to match the hole spacing (figure 3).
Pins which are too long should be clipped before soldering.
Iron soldering or dip soldering may be used as required.
The maximum soldering times for dip soldering are:
$t_{max} = 5$ s for 250° C solder temperature
$t_{max} = 12$ s for 300° C solder temperature

and for iron soldering:
$t_{max} = 15$ s for 250° C iron temperature
$t_{max} = 12$ s for 300° C iron temperature
$t_{max} = 8$ s for 350° C iron temperature

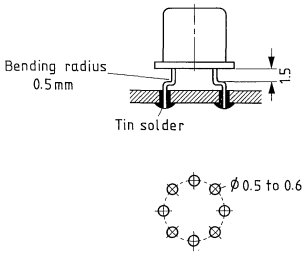


Figure 3

2.4 Protective measures for MOS circuits

Due to the sensitivity of MOS circuits to interference voltages and static charges, protective devices have been integrated into all inputs and outputs of the chips:

1. In the case of positive overvoltages, a p-n junction conducts in the forward direction to the substrate.
2. Negative overvoltages cause a defined diode breakdown with current limiting.
3. In addition, each input and output is connected to the gate and drain of a transistor with a threshold voltage of −35 Volt, so that these transistors short-circuit the inputs and outputs in the case of overvoltage.

In spite of these protective measures, it should be remembered that plastic floors, non-conductive working surfaces and chairs, and clothing containing synthetic fibers can lead to generation of charges which might endanger the circuits.

Machines and tools which come into contact with MOS circuits must have the same potential as these circuits. The working surface and all persons who handle MOS components should also be kept at the same potential.

In fabrication rooms, a relative humidity of approximately 70 % has proved to be a good additional protective measure for reducing static charges.

An air ionizer is recommended for preventing static charges in the case of automatic handling.

When MOS circuits are installed in equipment, the maximum ratings should be carefully observed. High resistance grounding of the solder bath or of the soldering iron should be provided. In the case of dip-soldering, care should be taken that excessive voltages differences in the solder bath are avoided.

In the case of p (n) channel MOS circuits, no positive (negative) voltages, referred to the substrate potential V_{SS}, may be connected to the pins.

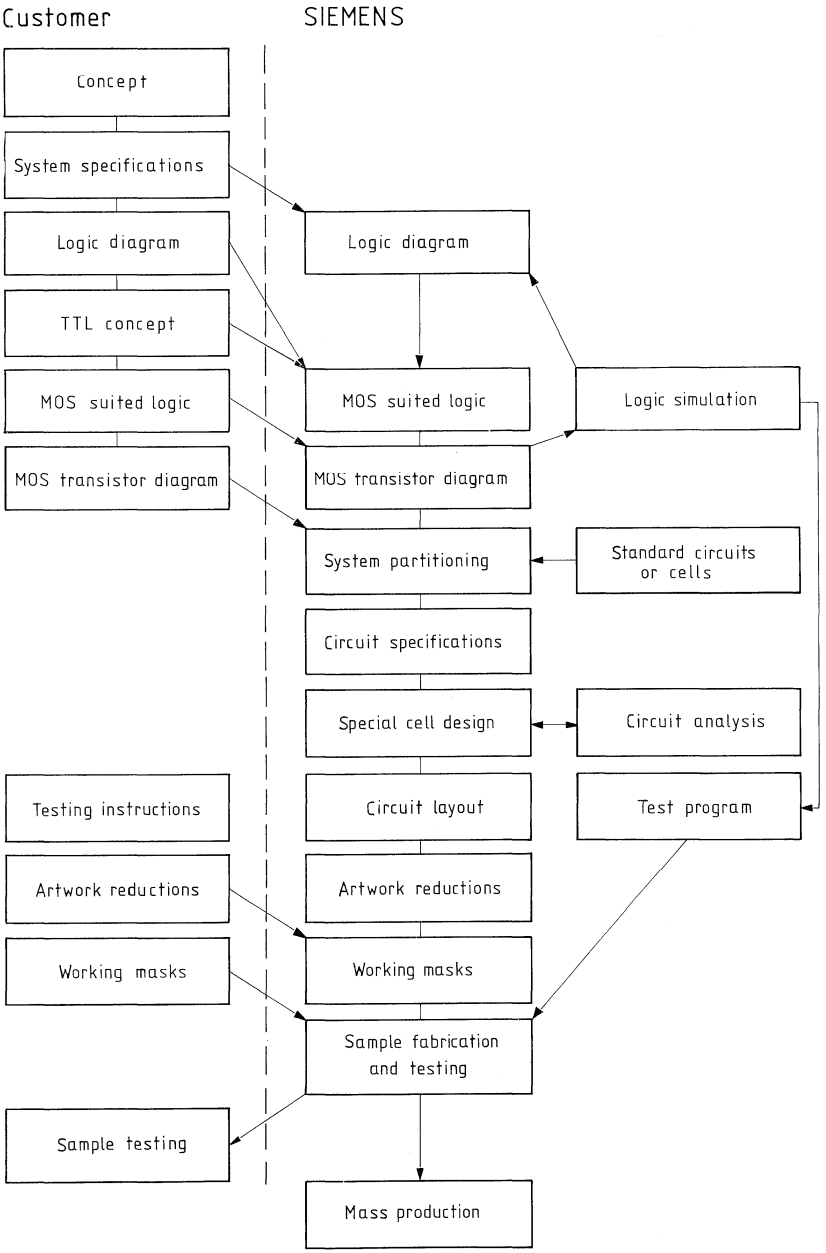
Protective measures for electrical operation

If, during electrical operation of MOS circuits, interference voltages occur and can reach the pins of the integrated circuits, then care must be taken that the maximum ratings of the voltage levels are not exceeded. In particular, the supply voltages V_{DD}-V_{SS} and V_{GG}-V_{SS} should be short-circuited by a capacitor with low impedance at high frequencies, installed in the immediate vicinity of the modules.

Interference voltages which could reach positive values with respect to V_{SS} must be limited by a suitable diode circuit.

Do not plug MOS circuits into their sockets or remove them while voltage is connected to the circuit.

Possible cooperation between customer and Siemens at various stages of development of a customer-specific circuit, using the example of an MOS device.



3. Data specifications

Maximum ratings

Maximum ratings are absolute limits. The integrated circuit may be destroyed if only a single value is exceeded.

Electrical characteristics

The electrical characteristics include the guaranteed distribution boundaries of the values which are maintained by the integrated circuit in the specified operating range.
The typical characteristics are mean values which are expected from fabrication. Unless otherwise specified, the typical characteristics are valid at $T_{amb} = 25°C$ and the specified supply voltage.

Characteristic functions

In the functional range, the functions shown in the circuit description will be fulfilled.

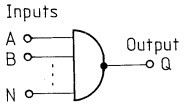
4. Logic data and symbols

4.1 Logic levels

In accordance with DIN 41785, part 4, for digital microcircuits, the two possible values of binary electrical digits are designated L (Low) and H (High). The values of the L range are defined as closer to $-\infty$, those of the H range as closer to $+\infty$. Similarly, the index A applies to the upper limit value (closer to $+\infty$) and index B to the lower limit value (closer to $-\infty$).
The previous logic symbols 0 and 1, or 0 and L or log. 0 and log. 1 are no longer used; specification of positive or negative logic is also no longer necessary.

4.2 Gate symbols

NAND gate

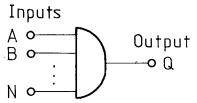


Truth table for a NAND gate with two inputs (e.g. 1/4 FZH 101).

Inputs A	B	Output Q
L	L	H
L	H	H
H	L	H
H	H	L

Logic function: $Q = \overline{A \wedge B \wedge \ldots \wedge N}$
Definition: An L signal will be present at the output only if A and B and ... and N have H signal.

AND gate

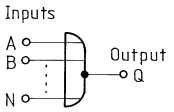


Truth table for an AND gate with two inputs (e.g. 1/4 FZH 251).

Inputs A	B	Output Q
L	L	L
L	H	L
H	L	L
H	H	H

Logic function: $Q = A \wedge B \wedge \ldots \wedge N$
Definition: An H signal will be present at the output only if A and B and ... and N have H signal.

NOR gate

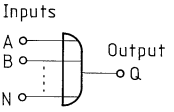


Truth table for a NOR gate with two inputs (e.g. 1/4 FZH 281).

Inputs A	B	Output Q
L	L	H
L	H	L
H	L	L
H	H	L

Logic function: $Q = \overline{A \vee B \vee \ldots \vee N}$
Definition: H signal will be present at the output only if A and B and ... and N have L signal.

OR gate

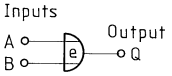


Truth table for an OR gate with two inputs (e.g. 1/4 FZH 291).

Inputs A	B	Output Q
L	L	L
L	H	H
H	L	H
H	H	H

Logic function: $Q = A \vee B \vee \ldots \vee N$
Definition: L signal will be present at the output only if A and B and ... and N have L signal.

Exclusive OR gate

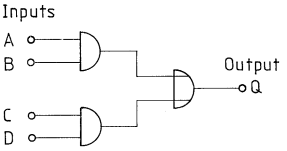


Truth table for an exclusive OR gate with two inputs (e.g. 1/4 FZH 271).

Inputs A	B	Output Q
L	L	L
L	H	H
H	L	H
H	H	L

Logic function: $Q = (A \wedge \overline{B}) \vee (\overline{A} \wedge \overline{B})$
Definition: H signal will be present at the output only if either only A or only B has H signal.

Inverting AND/OR gate

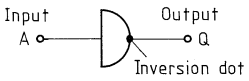


Logic function: $Q = (A \wedge B) \vee (C \wedge D)$

Truth table for an inverting AND/OR gate with 2 × 2 input (e.g. half FZH 151).

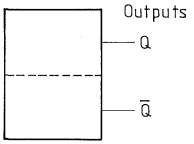
Inputs A	B	C	D	Output Q
L	L	L	L	L
H	L	L	L	L
L	H	L	L	L
H	H	L	L	H
L	L	H	L	L
H	L	H	L	L
L	H	H	L	L
H	H	H	L	H
L	L	L	H	L
H	L	L	H	L
L	H	L	H	L
H	H	L	H	H
L	L	H	H	H
H	L	H	H	H
L	H	H	H	H
H	H	H	H	H

Inverter

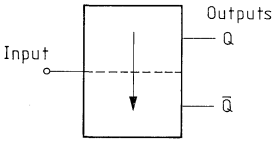


Logic function: $Q = \overline{A}$

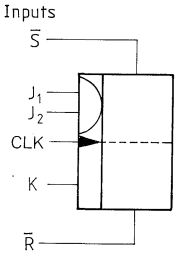
4.3 Flipflop symbols



Bistable circuit (flipflop) with complementary outputs



Monostable circuit (monoflop) with an input acting upon both outputs. The arrow indicates the output which is high when the circuit is stable.



J_1 J_2 and K are information inputs
J_1 and J_2 are AND-connected
J and K-inputs are gated by clock input CLK
$\overline{R}$ and $\overline{S}$ are independent reset and set inputs

Identification of dynamic inputs


Action at the output occurs when the input falls from H to L


Action at the output occurs when the input rises from L to H


Action while the input is high


Action while the input is low

4.4 Flipflop classification according to the logic function

D flipflop (delay flipflop)

The D flipflop has an input (indicated with a D) the logic state of which is transferred into the flipflop. It is controlled by a clock pulse. The information stored during the clock pulse is retained until the next clock pulse. Only then any new information is accepted by the D-input.

JK flipflop

The JK flipflop has information inputs indicated with a J and a K. They are gated by the clock input and determine the output state Q of the flipflop.
At J = L and K = L the Q-output is retained in its original state. At J = H and K = H the flipflop switches at every clock pulse to its complementary state (binary divider). Q = L results at J = L and K = H independent of the preceding output state. For J = H and K = L the defined output state ist Q = H.
Most JK flipflops have additional $\overline{R}$ and $\overline{S}$ inputs with which the flipflop can be operated independently of the clock pulse. In this way it is possible to select the initial state of the flipflop. $\overline{R}$ and $\overline{S}$ indicate that set or reset action is at L-level only.
The following tables show the function of the different types of flipflops.

Truth table for flipflops

Inputs		Output Q	
D or J	K	D flipflop	JK flipflop
L	L	L	Q_n
L	H		L
H	L	H	H
H	H		$\overline{Q}_n$
t_n		t_{n+1}	

Truth table for the $\overline{R}$ and $\overline{S}$ inputs of the flipflops

$\overline{R}$	$\overline{S}$	Q	$\overline{Q}$
L	H	L	H
H	L	H	L
L	L	undefined	
H	H	Q_n	$\overline{Q}_n$

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

5. Quality specifications

The quality of integrated circuits is specified as follows:

5.1 Maximum and minimum values of characteristics

5.2 Random sample agreement, AQL values (acceptable quality level)

A delivery batch whose defect percentage for a certain value is equal to or less than the specified AQL value will be accepted with high probability (above 90 %) during the appropriate random sample inspection with respect to this characteristic value.

The average defect percentage of delivered goods generally lies below the AQL value.

5.3 Classification of defects

A defect exists if a characteristic of a component does not comply with the specifications in the data sheet. The defects are divided into major and minor defects with respect to their seriousness, and into mechanical and electrical defects with respect to the type of defect. Unless otherwise specified, the AQL values summarized in Section 4 apply to the various defect classes. The identical random sample plan DIN 40080 (or) ABC-Std 105 are used as the basis for attribute inspection.

For each defect class for which an AQL value is specified, only the number of defective units (each with one or more defective characteristics) is evaluated in this defect class.

5.3.1 Division into defect classes

Depending on the probable effect of the defect on the application circuit, defects are divided into

Major defect class

If such a defect exists, the usability for the intended purpose is probably greatly reduced.

Minor defect class

If such a defect exists, the usability for the intended application is probably only slightly reduced.

5.3.2 Division according to defect type

A distinction is made between:

Defects in **mechanical characteristics**
(Package and leads)

Defects **in electrical characteristics**

Examples:

Major defects, mechanical characteristics
Broken connections or package, missing identification, wrong packages, bad cracks and cavities in the package, major surface defects, leads which cannot be soldered.

Minor defects, mechanical characteristics
Minor damage to the body surface, identification difficult to read, bent pins, incorrect dimensions.

Major defects, electrical characteristics
Malfunction, open circuit, short circuit, deviation from characteristic values by more than 50 %.

Minor defects, electrical characteristics
Minor deviations of voltages, currents, deviations from the dynamic characteristics, provided these have no major effect on the application.

5.4 AQL Table for digital integrated circuits

Defect type and defect class		AQL value
Bipolar circuits		
Mechanical defects	Sum of major and minor defects	0.65
	Major defects	0.25
Electrical defects	Sum of major and minor defects	0.65
	Major defects	0.15
MOS circuits		
Mechanical defects	Sum of major and minor defects	0.65
	Major defects	0.25
Electrical defects	Sum of major and minor defects	1.50
	Major defects	0.40
Switching times	ECL technology	0.65
	LSL technology	1.50

Test plan to DIN 40080 or ABC-Std 105 D, level II

Incoming inspection

The inspections carried out at the manufacturer's plant are intended to make incoming inspections unnecessary. If the buyer still wishes to carry out incoming inspection, the use of a random sample plan as shown in section 5 is recommended. The testing technology to be used must be agreed upon between the customer and the supplier.

The following details are necessary for assessment of any complaints:

Test circuit, random sample size, number of defective elements found, sample document, number of the packing slip.

5.5. Random sampling test plan for normal inspection
in accordance with DIN 40080 or ABC-Std 105 D, test level II

Lot size	Sample size	AQL-value 0.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5
		A R	A R	A R	A R	A R	A R	A R	A R	A R	A R	A R
2 to 8	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1
9 to 15	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↕
16 to 25	5	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓
26 to 50	8	↓	↓	↓	↓	↓	↓	↓	0 1	↓	↓	1 2
51 to 90	13	↓	↓	↓	↓	↓	↓	0 1	↕	↓	1 2	2 3
91 to 150	20	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4
151 to 280	32	↓	↓	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6
281 to 500	50	↓	↓	↓	0 1	↕	↓	1 2	2 3	3 4	5 6	7 8
501 to 1200	80	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11
1201 to 3200	125	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15
3201 to 10000	200	0 1	↕	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22
10001 to 35000	315	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↕
35001 to 150000	500	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↕
150001 to 500000	800	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↕	↕
500001 and more	1250	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↕	↕	↕

A = Number of acceptances; i.e. the maximum number of defective sample elements up to which the lot is accepted,

R = Number of rejections; i.e. the number of defective sample elements, at least achieved when the lot has been rejected.

Additional requirement

As the combination "Acceptance 0 and Rejection 1" has a low degree of significance the next larger sample size is to be used.

6. Summary of the symbols used

b	Pulse duration
B	Current gain
B	Bandwidth
C	Capacitance
C_I	Input capacitance
C_Φ	Input capacitance of the clock input
C_Q	Load capacitance at output
DI	Data input
DO	Data output
E	Enable
F_I	Input load factor
F_Q	Output load factor
F_{QH}	Output load factor, H signal
F_{QL}	Output load factor, L signal
f_I	Input frequency
f_Φ	Clock frequency
f	Maximum counter frequency
I_{DD}	Drain supply current
I_{GG}	Gate supply current
I_{tot}	Total current consumption
I_I	Input current
I_{IH}	H-input current
I_{IL}	L-input current
I_{N1}, I_{N2}	Input current at node N
I	Input
I_1	Input 1
I_2	Input 2
I_Q	Output offset current
I_Q	Short-circuit output current
I_{QH}	H-output current
I_{QL}	L-output current
I_{SH}	H-supply current
I_{SL}	L-supply current
O_S	Ground, earth
P	Power consumption
P_D	Idle consumption
P_{tot}	Total power consumption
P_Q	Output power
Φ	Clock input
Q	Output
$\overline{Q}$	Output, inverted

R	Resistance
R_G	Generator resistance
R_I	Input resistance
R_C	Collector load resistance
R_L	Load resistance
R_P	Adjustment resistance
$R_{thscase}$	Thermal resistance (system – case)
R_{thsamb}	Thermal resistance (system – ambient)
R_{QH}	H-output resistance
R_{QL}	L-output resistance
R_Q	Load resistance at output
R_Φ	Input resistance of clock input
T_{amb}	Ambient temperature
T_s	Storage temperature
T_{case}	Case temperature
T_j	Junction temperature
t_d	Pulse delay time
t_H	Hold time
t_I	Input pulse duration
t_n	Bit time before clock pulse
t_{n+1}	Bit time after clock pulse
t_P	Average signal propagation time
t_{PHL}	Signal propagation time (from H to L)
$t_{PHLR,S}$	Signal propagation time (set, reset input)
$t_{PHL\Phi}$	Signal propagation time (clock input)
t_{PD}	Pair-delay time
t_{pR}	Reset pulse duration
$t_{PR,S}$	Average signal propagation time (set, reset input)
t_{pS}	Set pulse duration
$t_{P\Phi}$	Average signal propagation time (clock input)
$t_{p\Phi}$	Clock pulse duration
t_{pC}	Counting pulse duration
t_T	Transmission time – t_r rise time, t_f fall time
t_r	Recovery time
t_Q	Output pulse duration
t_{THL}	Signal transition time (from H to L)
t_{TLH}	Signal transition time (from L to H)
$t_{THL\,Q}$	Signal transition time H-L of the output signal
$t_{TLH\,Q}$	Signal transition time L-H of the output signal
$t_{DHL\,Q}$	Delay time of the HL transition of the output signal
$t_{DLH\,Q}$	Delay time of the LH transition of the output signal
t_{DLH}	Delay time

t_S	Setup time
t_{SH}	H-setup time
t_{SHl}	H-setup time, left shift pulse
t_{SHr}	H-setup time, right shift pulse
t_{SL}	L-setup time
t_{SLl}	L-setup time, left shift pulse
t_{SLr}	L-setup time, right shift pulse
$t_{WH\,\Phi}$	H-pulse width of clock signal
$t_{WL\,\Phi}$	L-pulse width of clock signal
$t_{THL\,\Phi}$	Signal transition time H-L of the clock signal
$t_{TLH\,\Phi}$	Signal transition time L-H of the clock signal
$t_{DHL\,\Phi}$	Delay time of the HL transition of the clock signal
$t_{DLH\,\Phi}$	Delay time of the LH transition of the clock signal
$t_{WH\,I}$	Pulse width of the H input signal
$t_{WL\,I}$	Pulse width of the L input signal
$t_{THL\,I}$	HL transition time of the input signal
$t_{TLH\,I}$	LH transition time of the input signal
$t_{WH\,Q}$	Pulse width of the H output signal
t_W	Pulse width
V	Voltage, general
V_S	Supply voltage
V_{nm}	Noise margin
V_{SS}	Substrate supply voltage
V_{DD}	Drain supply voltage
V_{GG}	Gate supply voltage
V_{IH}	H-input voltage at information input
V_{IL}	L-input voltage at information input
V_{QH}	H-output voltage
$\overline{V_{QH}}$	Complement of output voltage V_{QH}
V_{QL}	L-output voltage
$\overline{V_{QL}}$	Complement of output voltage V_{QL}
$V_{\Phi H}$	H-input voltage at clock input
$V_{\Phi L}$	L-input voltage at clock input
V_{BE}	Base-emitter voltage
V_{DI}	Differential input voltage
V_{cm}	Input common mode voltage
V_n	Noise voltage
V_F	Functional range
V_I	Input voltage at information input
V_R	Reset voltage
Z_I	Input impedance
Z_Q	Output impedance
TC	Temperature coefficient

LSL Series

General information on the LSL series FZ 100

FZ 100 is a low-speed noise-immune logic series of monolithic integrated circuits. A Z diode input as well as a relatively large collector capacitance of the input transistor ensure an excellent static and dynamic noise immunity of the integrated circuit. Propagation delay times can be adjusted with capacitors. Thus the dynamic noise immunity can be increased as required. Due to these advantages, the series FZ 100 is in particular suited for applications where strong noise endangers operations, and where the noise immunity is much more important than the switching speed.

1. Noise immunity

1.1 Static noise immunity

The static noise immunity characterizes the behavior of a system disturbed by noise pulses which last longer than the average propagation delay time. The static noise immunity defines the voltage levels which do not influence the logic state. The typical values of the static noise immunity or noise margin are derived from the transfer function (figure 5).
For the L state follows:

at $V_S = 12\,V$: $V_{nmL} = V_{T1} - V_{IL} = 5.9 - 0.9 = 5.0\,V$
at $V_S = 15\,V$: $V_{nmL} = V_{T2} - V_{IL} = 5.6 - 0.9 = 4.7\,V$.

For the H state follows:
at $V_S = 12\,V$: $V_{nmH} = V_{OH} - V_{T1} = 11.3 - 5.9 = 5.4\,V$
at $V_S = 15\,V$: $V_{nmH} = V_{QH} - V_{T2} = 14.3 - 5.6 = 8.7\,V$

The guaranteed noise immunity under worst-case conditions results as follows:
$V_{nmL} = V_{IL} - V_{QL} = 4.5 - 1.7 = 2.8\,V$ at $V_S = 12$ and $15\,V$
$V_{nmH} = V_{QH} - V_{IH} = 10 - 7.5 = 2.5\,V$ at $V_S = 12\,V$ and
$V_{nmH} = V_{QH} - V_{IH} = 12 - 7.5 = 4.5\,V$ at $V_S = 15\,V$.

1.2 Dynamic noise immunity

The dynamic noise immunity characterizes the behavior of a system disturbed by noise pulses of a shorter duration than the signal propagation delay time. In this case the energy of the noise pulse – pulse amplitude and duration – determines whether a change of the logic state will take place.
The practical aspects of the dynamic noise immunity are the input noise immunity and the immunity against capacitively coupled noise. The source of capacitively coupled noise can either be cross talk (system noise) or foreign noise. A coupling capacitance of up to 1.6 nF typically does not introduce any cross talk. Due to this value, system noise can in general be regarded as being a minor problem, and foreign noise sources only have to be considered as important.
The following figures show the noise immunity of the transistor-transistor logic TTL, the complementary MOS-logic CMOS, and the low-speed noise-immune logic LSL.

1.2.1 Input noise immunity

Pulse duration and amplitude of a noise pulse are limited by the propagation delay time t_P of a gate. The noise amplitude may become greater than the static noise immunity if the noise pulse duration $b \leqq \frac{1}{2}\, t_P$. The noise amplitude may not exceed the static noise immunity if $b \geqq t_P$. However, t_P can be adjusted as required by the integrating capacitance C_N.

Figures 1 and 2 show the typical input noise immunity of NAND gates with and without integrating capacitance at supply voltages V_S = 12 V. The noise voltage V_{nm} is shown as a function of the noise pulse duration b. Figure 2 indicates the more critical case where an L signal at the input is disturbed. This is due to the transition time t_{THL} being shorter than t_{TLH}. Thus the noise pulse duration at L state is less than at H state.

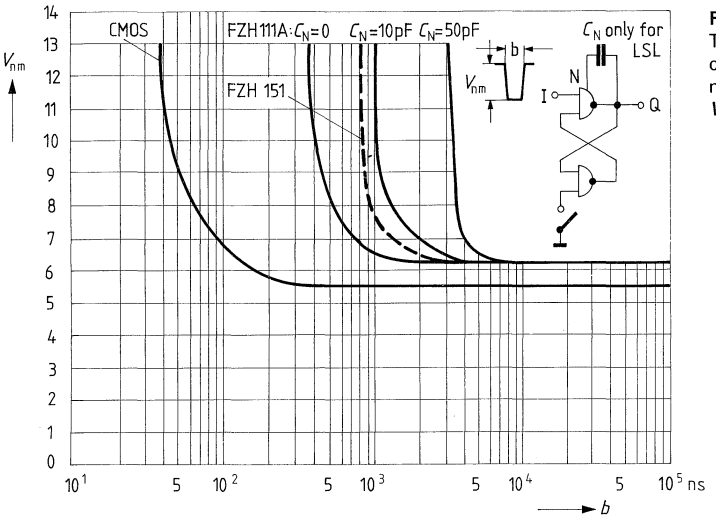


Figure 1
Typical limit characteristics for input noise at H state
$V_{nm} = f(b)$ at V_S = 12 V

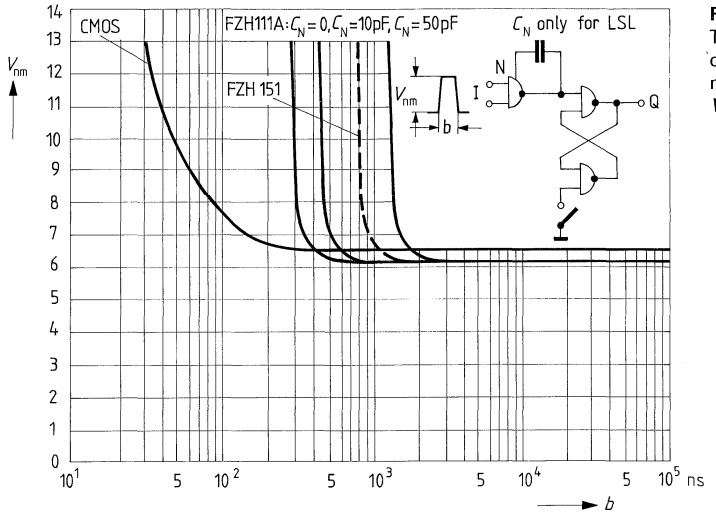


Figure 2
Typical limit characteristics for input noise at L state
$V_{nm} = f(b)$ at V_S = 12 V

1.2.2 Capacitive noise coupling

For capacitive coupling of noise, the LSL modules have the advantage of a low impedance push-pull output, with a value of approximately 20 Ω in the L state and approximately 300 Ω in the H state. This results in a small time constant, causing rapid decay of the noise pulses. Figures 3 and 4 show the sensitivity of the L and H states to capacitive noise coupling for NAND gates with and without integrating capacitance C_N. The typical permissible noise voltage V_{nm} is shown as a function of the coupling capacitance C_S. The more critical case is where noise disturbs the H signal, as the gate output has a higher internal resistance in the H state than in the L state. The transition time of the noise source was approximately 1 ns and the source resistance was approximately 1 Ω.

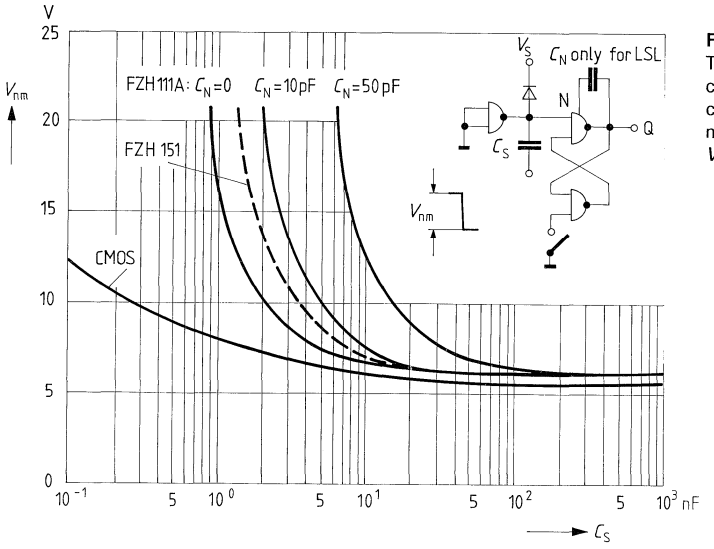


Figure 3
Typical limit characteristics for capacitively coupled noise at H state
$V_{nm} = f(C_S)$ at $V_S = 12$ V

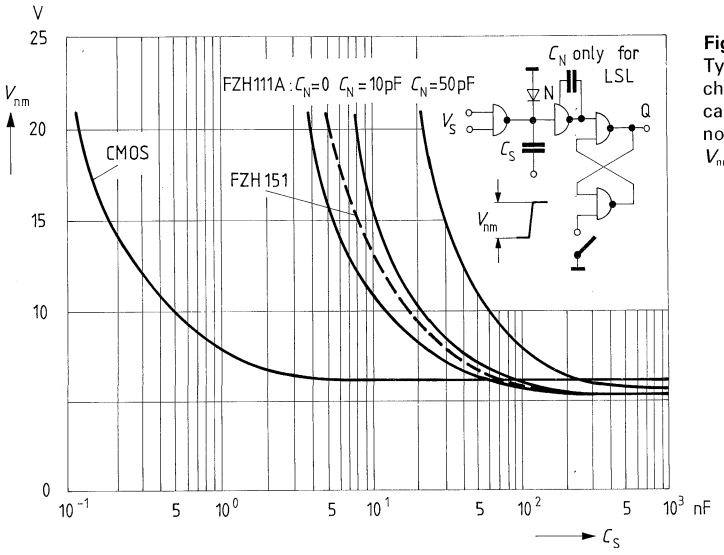


Figure 4
Typical limit characteristics for capacitively coupled noise at L state
$V_{nm} = f(C_S)$ at $V_S = 12\,V$

1.3 Destruction energy

The amount of energy which is permissible at any terminal of an LSL circuit without danger of destruction is typically 1 mWs per circuit. Suitable protection is possible with the aid of 2 diodes to ground and supply voltage or 1 Z diode and 1 series resistor. The IC FZH 301/305 is suitable for special applications where the danger of destruction is great.

2. Static data

2.1 Maximum ratings

Maximum ratings are absolute limits. The integrated circuit may be destroyed if a single value is exceeded. Unless otherwise specified, maximum ratings are valid at $T_{amb} = 25°C$.

2.2 Electrical characteristics

Typical characteristics are statistical mean values which are supplemented by a guaranteed deviation (worst case). Unless otherwise specified, they are valid at the supply voltage $V_S = 12\,V$ or 15 V and at an ambient temperature $T_{amb} = 25°C$.

2.3 Characteristics

2.3.1 Transfer characteristics

Figure 5 shows the transfer characteristics $V_Q = f(V_I)$ of NAND gates at supply voltages V_S of 12 V and 15 V. They depend only slightly on the output load. Different output load factors at L and H make it possible to connect unused outputs in parallel in order to avoid undesirable noise pickup. Inputs connected in parallel, load the output additionally with the diode current only in the H state.
In order to ensure reliable operation, the input voltage must reach a specific voltage level (threshold value). This threshold value is determined graphically at the intersection of the transfer characteristic with the straight line $V_I = V_Q$.

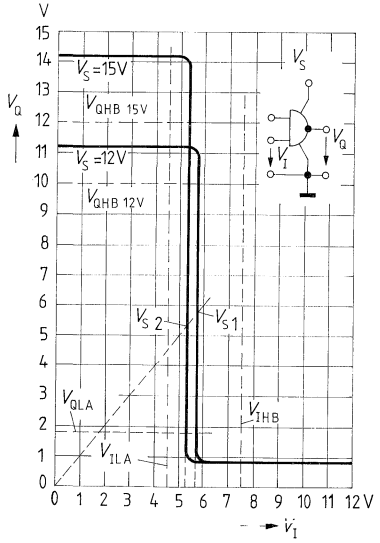


Figure 5
Typical transfer characteristics of a gate
$V_Q = f(V_I)$ at $V_S = 12$ and 15 V

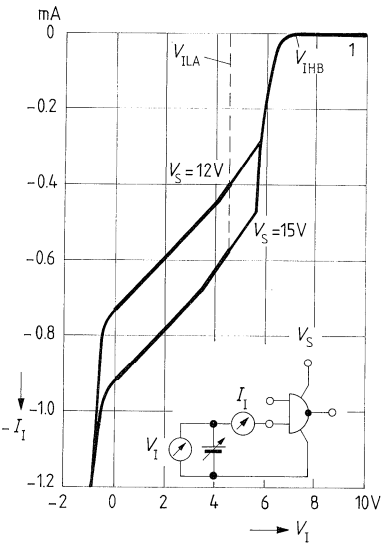


Figure 6
Typical input characteristic
$I_I = f(V_I)$ at $V_S = 12$ and 15 V

2.3.2 Input characteristic

Figure 6 shows the input characteristic $I_I = f(V_I)$ for the two supply voltages $V_S = 12$ V and 15 V. This characteristic can be divided into three ranges:

1. If H level is applied to the input, only a small reverse current (approx. 1 µA) flows into the input. The breakdown voltage of the diodes is >18 V or >30 V, respectively, for the B and S types, and may not be exceeded.
2. If L is applied to the input, the input current flows out of the input.
3. In the case of negative input voltages, the substrate diodes at the input conduct, causing a rapid increase in the input current. As differing maximum permissible negative values apply to the various devices, these are specified in detail in the maximum ratings.

The input characteristics are independent of the output load, as there is no feedback to the input. The TTL-LSL level converter FZH 181 has an input characteristic similar to that of TTL circuits.

2.3.3 Output characteristics

Figure 7 shows the output characteristic $V_{QL} = f(I_{QL})$ in the L state for normal outputs and power outputs at the supply voltage $V_S = 12$ V and 15 V. The current I_{QL} flows into the gate output.

This typical characteristic shows that the output current may exceed the load current $I_{QL} = 15$ or 18 mA, respectively, at $F_Q = 10$ and at the maximum output voltage $V_{QL} = 1.7$ V specified in the data sheet. However, care must be taken that the total power dissipation of 500 mW per package is not exceeded.

Figures 8 and 8a show the output characteristics in the H state $V_{QH} = f(I_{QH})$. In this case, the current I_Q flows out of the gate output. Simultaneous short-circuiting of several outputs of one package is not permitted. The maximum short-circuit duration is one second for ICs without short-circuit protection. In the case of ICs with short-circuit protection, a continuous short circuit is not permitted. Compliance with these rules will avoid overloading of the ICs.

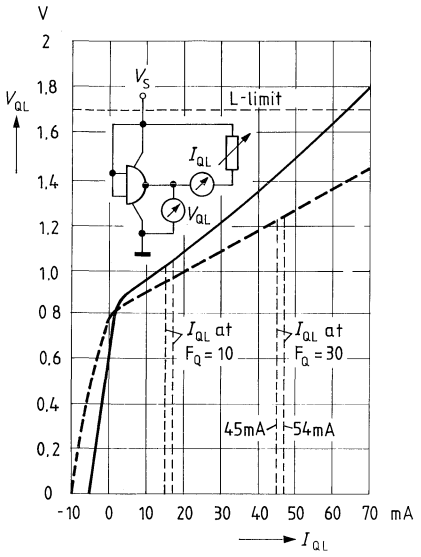


Figure 7
Typical output characteristic at the L state
$V_{QL} = f(I_{QL})$ at $V_S = 12$ and 15 V
– – – = FZH 141/5

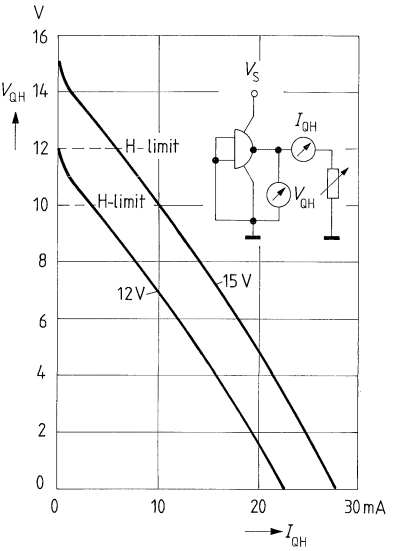


Figure 8
Typical output characteristic at the H state
$V_{QH} = f(I_{QH})$ at $V_S = 12$ and 15 V

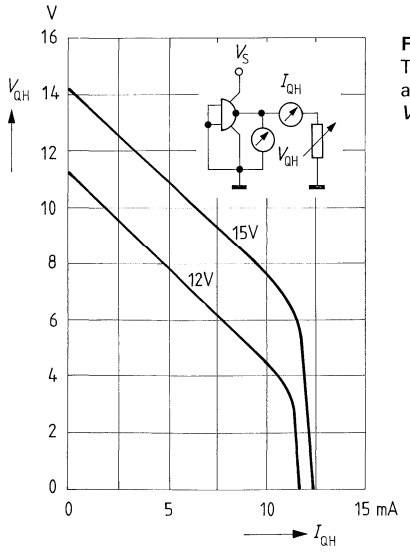


Figura 8a
Typical output characteristic at the H state
$V_{QH} = f(I_{QH})$ at $V_S = 12$ and 15 V

Figure 8 applies to:

FZH 121/125
FZH 131/135
FZH 141/145
FZH 171/175
FZJ 101/105
FZJ 111/115

Figure 8a applies to:

FZH 101/105 A
FZH 111/115 A
FZH 191/195
FZH 201/205
FZJ 121/125
FZJ 131/135
FZJ 141/145 A
FZJ 151/155 A
FZJ 161/165

2.4 Logic data

2.4.1 Input load factor

The input load factor defines the currents required by a single input at H state as well as L state. The upper limit of the H input current per input is $I_{IHA} = 1\ \mu A$. The upper limit of the L input current per input is $I_{ILA} = -1.5$ mA at $V_S = 12$ V and -1.8 mA at $V_S = 15$ V. These values define the normalized load factor $F_I = 1$. They are valid within the entire temperature range. $F_I = 2$ means for example an L input current of $-I_{IL} = 2 \times 1.5 = 3$ mA at $V_S = 12$ V and $-I_{IL} = 2 \times 1.8 = 3.6$ mA at $V_S = 15$ V and an H input current of $I_{IH} = 2 \times 1 = 2\ \mu A$.

2.4.2 Output load factor

The output load factor defines how many normalized loads $F_I = 1$ can be driven by a single output. The H output load factor is higher than the L output load factor. In this way it is possible to connect unused inputs of the same gate in parallel without accounting for an additional load.

3. Dynamic data

3.1 Load capacitance

Figure 9 shows the influence of capacitive loading on the switching parameters. It can be seen that the switching parameters are nearly independent of the load capacitance. This is due to a low output resistance at the L state as well as the H state. In this way it is possible to use long connection lines which essentially represent a capacitive load. The switching parameters remain constant over a wide range.

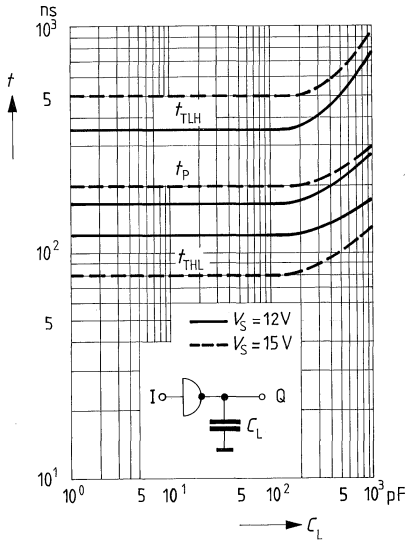


Figure 9
Typical switching parameters versus load capacitance $t = f(C_L)$
t_T = transition time, t_P = propagation delay

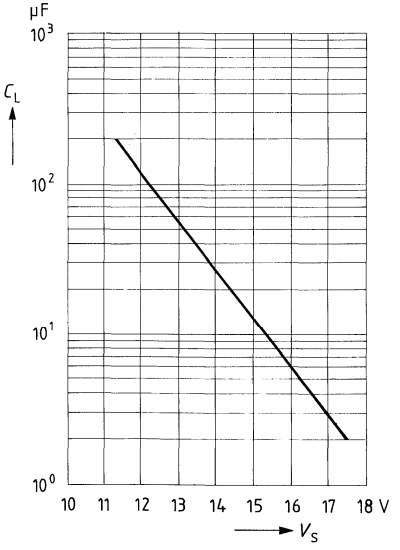


Figure 9a
Permissible load capacitance $C_L = f(V_S)$

3.2 Delay capacitance

Due to a special geometry of the input transistor the collector capacitance is relatively great. This causes long propagation delay times and a high dynamic noise immunity results. Circuits with an N node enable the designer to lengthen the propagation delay times with an integrating capacitor C_N. Thus the dynamic noise immunity can be adapted as required. The capacitor is connected between output Q and N node with gates. The flipflops FZJ 101/105 require two capacitors to delay the slave. One between output Q and node N_Q and another one between output $\overline{Q}$ and node $N_{\overline{Q}}$. Two additional capacitors may be provided at the nodes N_J, N_J and N_K, N_K of the flipflops FZJ 111 and FZJ 115 to increase the noise immunity of the master. No limit is given for the integrating capacitance for gates and flipflops.
C_N must be connected between the N input and ground O_S with the circuits FZK 101/105, FZJ 141/145 A, FZJ 151/155 A, and FZJ 161/165. The upper limit of C_N is 500 pF for the FZK 101/105 and 1 nF for the remaining circuits.
Figure 10 shows the switching parameters versus the capacitance C_N for gates at supply voltages V_S = 12 V and 15 V.

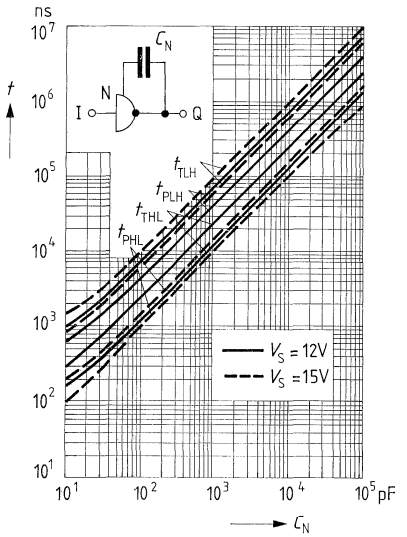
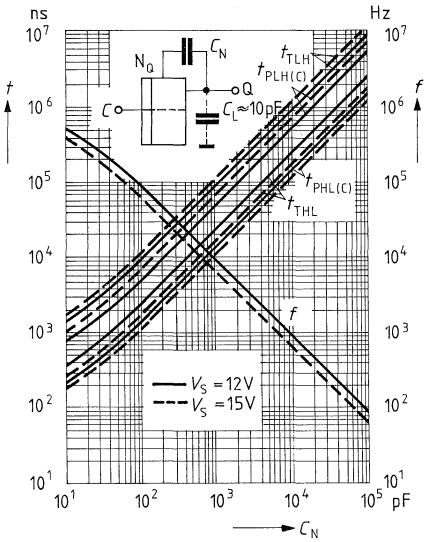
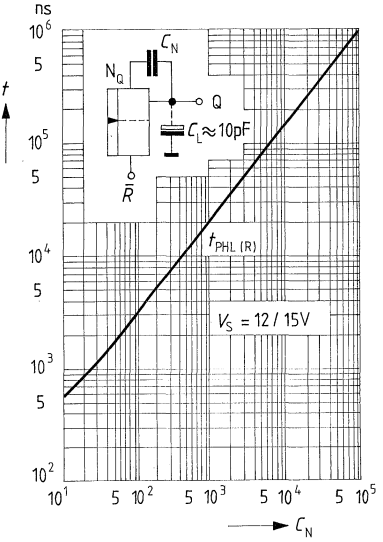


Figure 10
Typical switching parameters of gates versus the integrating capacitance
$t = f(C_N)$,
t_T = transition time
t_P = propagation delay

Figures 11 and 12 show the typical switching parameters for flipflops between clock input CLK and output Q as well as the reset input $\overline{R}$ and Q versus the integrating capacitance C_N at supply voltages V_S = 12 V and 15 V.





Figures 11 and 12
Typical switching parameters of flipflops versus the integrating capacitance $t = f(C_N)$.
t_T = transition time, t_P = propagation delay

The characteristics are referred to the Q output only. Identical results will be achieved for measurements between CLK and output $\overline{Q}$ and the set input $\overline{S}$ and $\overline{Q}$. The maximum clock frequency f can directly be derived from the switching parameters as shown in fig. 11. The integrating capacitance also determines the duty cycle of the clock pulse. While the clock pulse duration $t_{pH(C)}$ depends on the capacitance at the master, the clock pause $t_{pL(C)}$ is defined by the capacitance at the slave. The corresponding diagram is shown in figure 13.
The actual duty cycle is given by the formula:

$$t_p = t_{pL(C)} + t_{pH(C)}$$

As no integrating capacitance is provided at the master of the FZJ 101/105, the minimal value of the clock pulse duration has to be inserted.

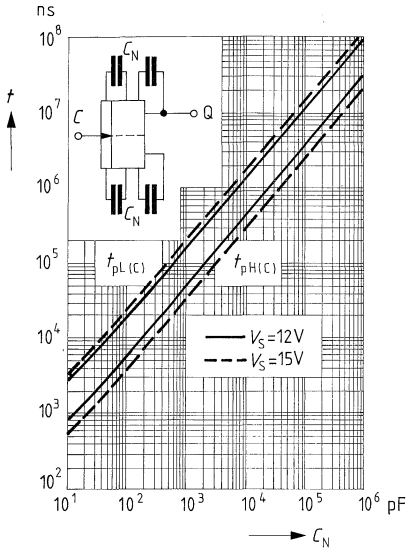


Figure 13
Typical duty cycle of the clock pulse versus the integrating capacitance $t_p = f(C_N)$

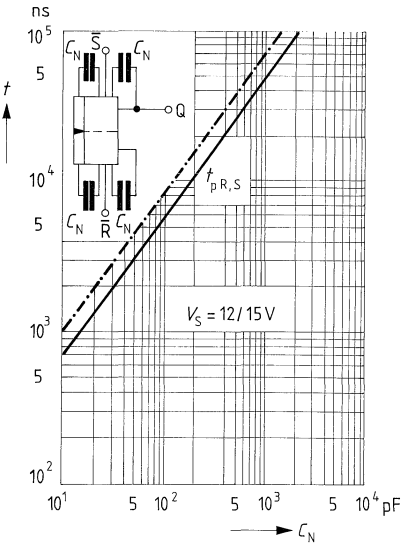


Figure 14
Typical (——) and minimal (– · –) set and reset pulse duration versus the integrating capacitance $t_p = f(C_N)$

Figure 14 shows the required increase of the set and reset pulse duration versus the integrating capacitance C_N at supply voltages V_S = 12 V and 15 V. No integrating capacitance is provided at the master of the FZJ 101/105. Thus the diagram applies only at CLK = H, when master and slave are disconnected.

3.3 Switching times

The signal propagation delay time t_{PLH} specifies the pulse delay between the input and output voltages when the output switches from L to H signal. Correspondingly, the propagation delay time t_{PHL} applies when the output switches from H to L. Measurement of the propagation times is referred to the 4.5 V levels.
The signal transition times t_{TLH} and t_{THL} of the output pulses are measured between the 10 % and 90 % points. The pair delay defines the signal delay which is caused by two inverting gates connected in series. This results in an output signal which is in phase with the input signal, but delayed by the time $t_P = t_{PLH} + t_{PHL}$.

Figures 15 to 19 show the signal propagation delay times as well as the transition time versus the supply voltage V_S over the operating range of 11.4 to 17 V.

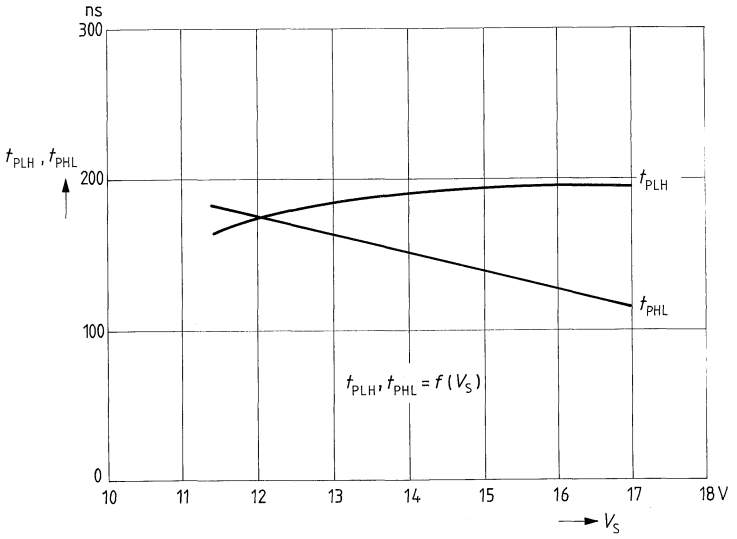


Figure 15
Propagation delay time $t_{PLH} = f(V_S)$
Propagation delay time $t_{PHL} = f(V_S)$
for NAND gates

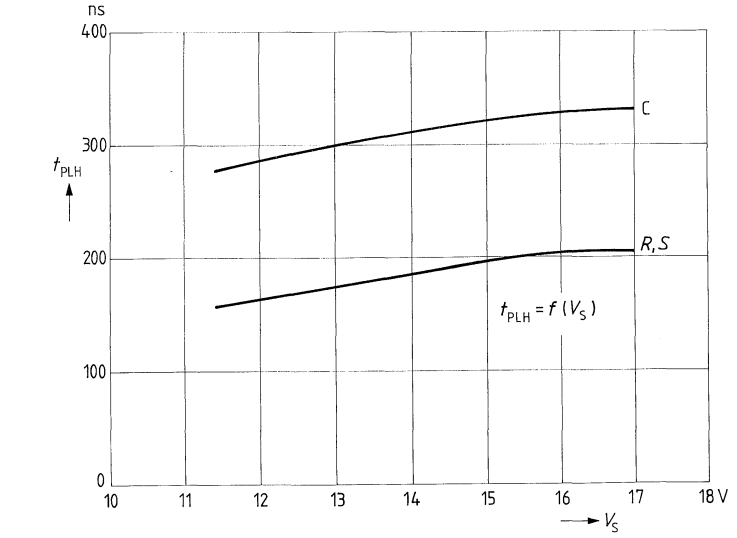


Figure 16
Propagation delay time $t_{PLH} = f(V_S)$
for flipflops

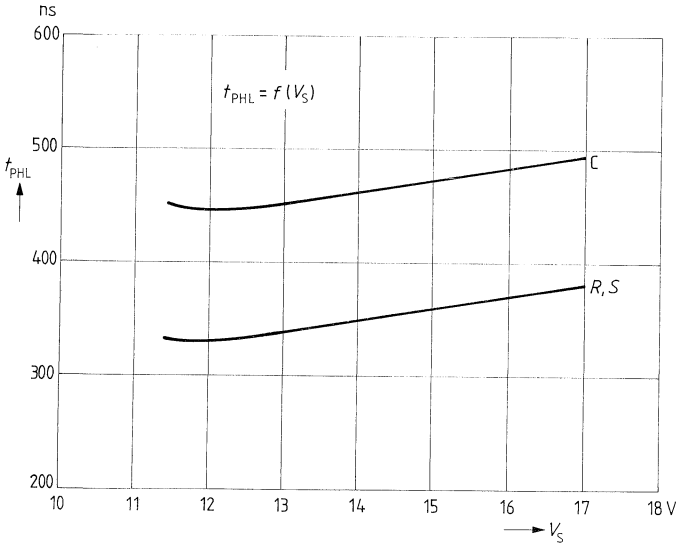


Figure 17
Propagation delay time
$t_{PHL} = f(V_S)$
for flipflops

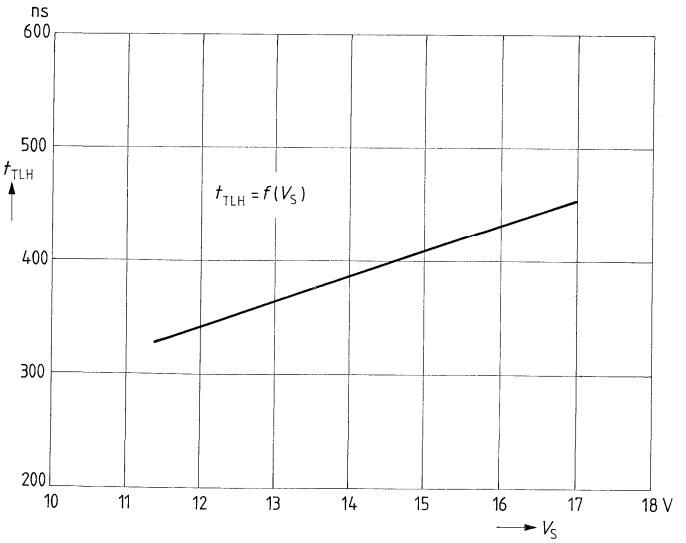


Figure 18
Transition time
$t_{TLH} = f(V_S)$
for NAND gates and flipflops

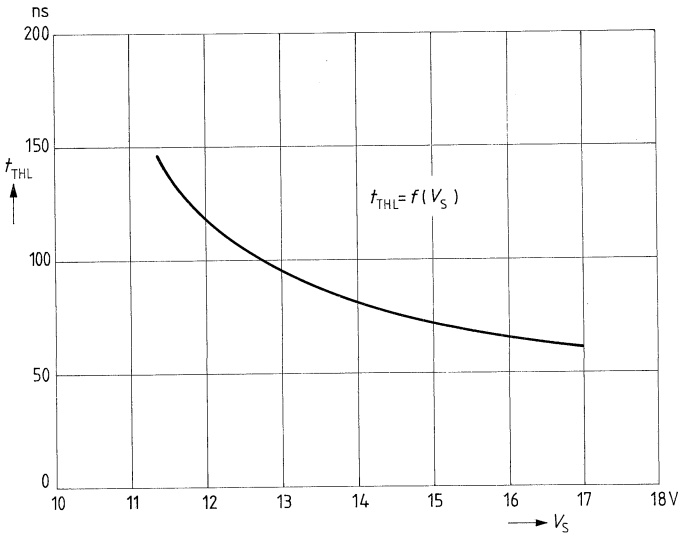


Figure 19
Transition time
$t_{THL} = f(V_S)$
for NAND gates and flipflops

4. Electrical characteristics

The electrical characteristics in the tables are given for two supply voltage ranges. The limits of the 12 V range are $V_{SB} = 11.4$ V and $V_{SA} = 13.5$ V. The limits of the 15 V range are $V_{SB} = 13.5$ V and $V_{SA} = 17$ V. For the B types, the maximum input voltage and the maximum output voltage with an open collector is $V_I = V_Q \geqq 30$ V. For the S types, the maximum supply voltage is $V_S \geqq 30$ V. The typical values are valid at the appropriate nominal voltages and at an ambient temperature $T_{amb} = 25°C$. Additional limits are defined separately for the ICs FZH 211 S and FZH 301/305.

Maximum ratings

			Lower limit B	Upper limit A	Unit
Supply voltage	FZH 181/185	V_S	0	7	V
	all other types	V_S	0	18	V
	S types	V_S	0	30	V
Input voltage	FZH 181/185	V_I	0	5.5	V
	all other types	V_I	0	18	V
	B and S types	V_I	0	30	V
Voltage at node N		V_N	−1	0.6	V
Current at node N		I_N	−10	2	mA
Ambient temperature	range 1	T_{amb}	0	70	°C
	range 5	T_{amb}	−25	85	°C
Storage temperature		T_s	−65	125	°C

Maximum ratings, maximum negative values at $T_{amb} = 0$ to 70° C

	V_I(V)	I_I(mA)	at V_S(V)
All inputs except N nodes, and N_I pins, as well as except FZH 151/155, FZH 181/185		−25	17
FZH 151/155	−0.7		17
FZH 181/185	−0.5	−25	5

Application notes:

Unused pins shown in the pin configuration must be left open.

The rise and fall times of the input signals of ICs without C_N should generally not be less than 1 V/µs. When changing from delayed circuits to undelayed circuits, care must be taken that the transition times are shortened sufficiently. Leads to the N nodes must be kept as short as possible.

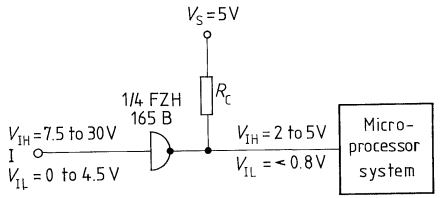
LSL circuits for input voltages up to 30 V, B series

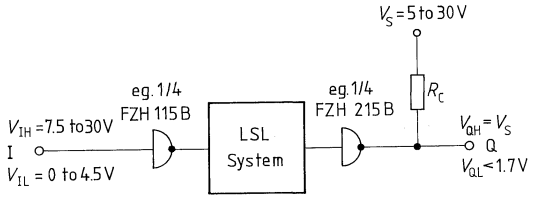
A number of LSL circuits are now available with an input voltage rating ≦ 30 V, and, in the case of open collector output currents, for output voltages ≦ 30 V. This makes it possible to connect the LSL series directly, without interface circuits, to systems using 24 V or 28 V levels. The LSL-TTL level converter FZH 165 B is of particular importance because it can be used as a converter from systems with input voltages ≦ 30 V to 5 V systems, such as microprocessors, silicon gate MOS and TTL.

Available types

Type	Ordering code	Function
FZH 115 B	Q67000-H215-B	Quad NAND gate with $V_I \leqq 30$ V
FZH 165 B	Q67000-H289-B	LSL-TTL level converter for $V_I = V_Q \leqq 30$ V
FZH 215 B	Q67000-H640-B	Quad NAND gate for $V_I = V_Q \leqq 30$ V
FZH 245 B	Q67000-H646-B	Dual NAND Schmitt trigger for $V_I \leqq 30$ V
FZH 255 B	Q67000-H818-B	Quad AND gate for $V_I \leqq 30$ V
FZH 265 B	Q67000-H820-B	Dual NAND gate and quad inverter for $V_I \leqq 30$ V
FZH 285 B	Q67000-H824-B	Quad NOR gate for $V_I \leqq 30$ V
FZH 295 B	Q67000-H826-B	Quad OR gate for $V_I \leqq 30$ V
FZH 301	Q67000-H1586	Quad NOR gate for $V_I \leqq 30$ V
FZH 305	Q67000-H1587	Quad NOR gate for $V_I \leqq 30$ V

Application examples





Type	Ordering code
FZH 121	Q67000-H192
FZH 125	Q67000-H254
FZH 131	Q67000-H193
FZH 135	Q67000-H255
FZH 171	Q67000-H328
FZH 175	Q67000-H329

FZH 101 A, FZH 105 A: Quad 2-input NAND gate
FZH 111 A, FZH 115 B: Quad 2-input NAND gate with N-input } see FZH 191
FZH 121, FZH 125: Dual 5-input NAND gate
FZH 131, FZH 135: Dual 5-input NAND gate with N-input
FZH 171, FZH 175: Dual 4-input NAND gate with expander nodes N_1 and N-input

Electrical characteristics, 12 V range
Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ and V_{SB}	2			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA} $V_{IL} = 4.5\,V$ $-I_{QH} = 0.1\,mA$	2	10	11.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5\,V$ $I_{QL} = 15\,mA$	1		0.9	1.7	V
DC noise margin							
H-signal	V_{nm}			2.5	5		V
L-signal	V_{nm}			2.8	5		V
H-input current, each input	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	3			1	µA
L-input current, each input	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$	4		0.8	1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_I = 0\,V$	5	10	30	50	mA
H-supply current, each gate	I_{SH}	$V_S = V_{SA}$, $V_I = 0\,V$	6		0.9	1.6	mA
L-supply current, each gate	I_{SL}	$V_S = V_{SA}$, $V_I = V_{IHA}$	7		1.7	3	mA
Power consumption, each gate	P	$V_S = V_{SA}$ duty cycle 1:1			16	31	mW

Delay times, $V_S = 12\,V$, $F_Q = 1$, $T_{amb} = 25°C$

Propagation delay	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	26	90	175	310	ns
	t_{PHL}			90	175	310	ns
Transition time	t_{TLH}	$C_L = 10\,pF$		200	340	570	ns
	t_{THL}			70	120	210	ns

Electrical characteristics, 15 V range

Temperature range 1 and 5

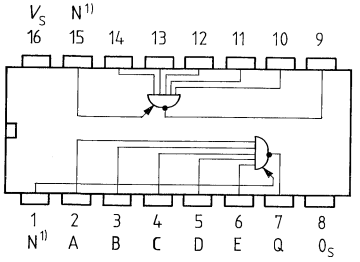
		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			13.5	15	17	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}	2			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA}, $V_{IL} = 4.5\,V$, $-I_{QH} = 0.1\,mA$	2	12	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5\,V$, $I_{QL} = 18\,mA$	1		1	1.7	V
DC noise margin							
H-signal	V_{nm}			4.6	8		V
L-signal	V_{nm}			2.8	5		V
H-input current, each input	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	3			1	µA
L-input current, each input	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$	4		1	1.8	mA
Short-circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_I = 0\,V$	5	15	37	60	mA
H-supply current, each gate	I_{SH}	$V_S = V_{SA}$, $V_I = 0\,V$	6		1.2	2.1	mA
L-supply current, each gate	I_{SL}	$V_S = V_{SA}$; $V_I = V_{IHA}$	7		2.3	4	mA
Power consumption, each gate	P	$V_S = V_{SA}$ duty cycle 1:1			27	52	mW

Delay times, $V_S = 15\,V$, $F_Q = 1$, $T_{amb} = 25°C$

Propagation delay	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	26		195		ns
	t_{PHL}				140		ns
Transition time	t_{TLH}	$C_L = 10\,pF$			410		ns
	t_{THL}				75		ns

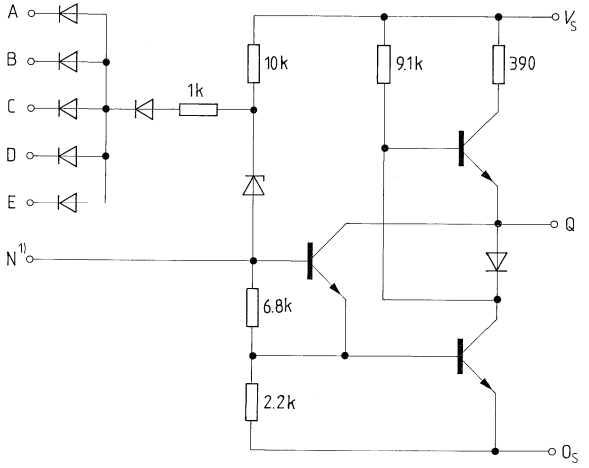
Dual 5-Input NAND-Gate

FZH 121
FZH 125
FZH 131
FZH 135



Pin configuration
top view

Schematic (one gate)

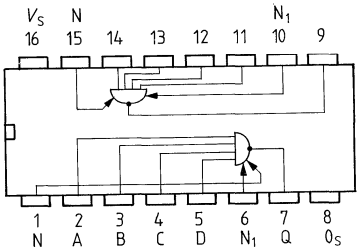


Logic data, each gate		Upper limit A
H-output load factor	F_{QH}	100
L-output load factor	F_{QL}	10
Input load factor, each input	F_I	1

Logic function $Q = \overline{A \wedge B \wedge C \wedge D \wedge E}$

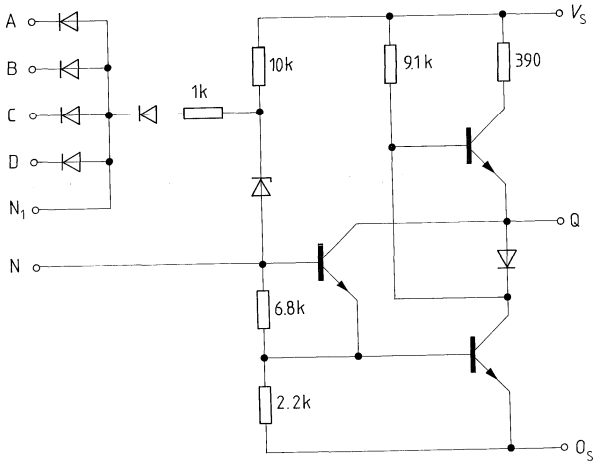
[1)] FZH 131/135 only

The number of inputs can be expanded as required by means of additional input diodes BAW 76 at the expander inputs N_1. The anodes of the diodes must be connected in parallel to N_1.



Pin configuration
top view

Schematic (one gate)



Logic data, each gate		Upper limit A
H-output load factor	F_{QH}	100
L-output load factor	F_{QL}	10
Input load factor, each input	F_I	1

Logic function $Q = \overline{A \wedge B \wedge C \wedge D \wedge N_1}$

Type	Ordering code
FZH 141	Q67000-H194
FZH 145	Q67000-H256

The electrical characteristics of the FZH 141/145 are similar to the FZH 131/135 except of the values stated below.

Electrical characteristics, 12 V range
Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5$ V $I_{QL} = 45$ mA	1		1.3	1.7	V

Electrical characteristics, 15 V range
Temperature range 1 and 5

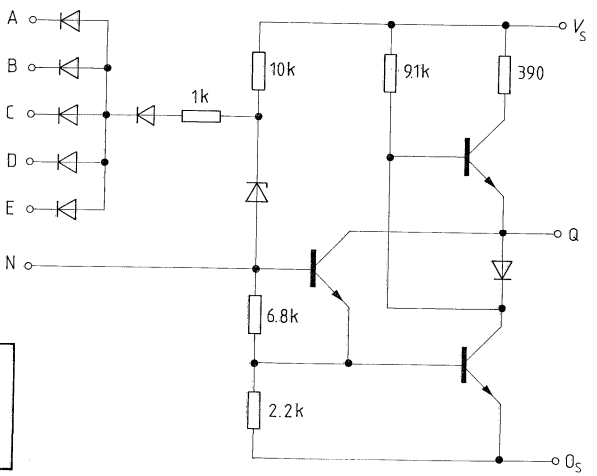
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5$ V $I_{QL} = 54$ mA	1		1.4	1.7	V

Logic data, each gate

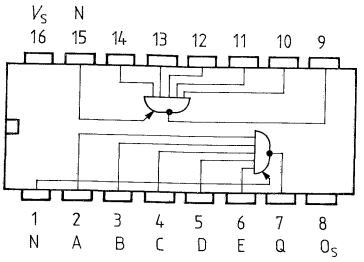
H-output load factor	F_{QH}					100	
L-output load factor	F_{QL}					30	
Input load factor, each input	F_I					1	

Logic function $Q = \overline{A \wedge B \wedge C \wedge D \wedge E}$

Schematic (one gate)



Pin configuration
top view



Type	Ordering code
FZH 151	Q 67000-H195
FZH 155	Q 67000-H260

The FZH 151 and FZH 155 are AND-OR gates suited for the following applications: Flipflop, counter, divider, shift register, adder, delay element. The lower limit of the supply voltage is $V_S = 10\,V$.

Electrical characteristics, 12 V range
Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	15	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$	16			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$, $V_{IL} = 4.5\,V$, $-I_{QH} = 0.1\,mA$	16	10	11.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5\,V$, $I_{QL} = 30\,mA$	15		0.9	1.7	V
DC noise margin							
H-signal	V_{nm}			2.5	5		V
L-signal	V_{nm}			2.8	5		V
H-input current at R_1, C_1, R_2, C_2	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	17			2	µA
H-input current remaining inputs	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	17			1	µA
L-input current at R_1, C_1, R_2, C_2	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$	18		1	2.5	mA
L-input current remaining inputs	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$	18		0.5	1.25	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_I = 0\,V$	19	10	30	50	mA
H-supply current	I_{SH}	$V_S = V_{SA}$, $V_I = 0\,V$	20		14	22	mA
L-supply current	I_{SL}	$V_S = V_{SA}$, $V_I = V_{IHA}$	21		8	15	mA
Power consumption	P	$V_S = V_{SA}$, duty cycle 1:1			132	250	mW

Delay times, $V_S = 12\,V$, $F_Q = 1$, $T_{amb} = 25°C$

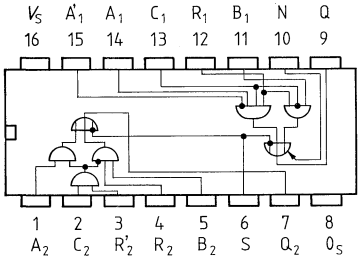
		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Propagation delay	$t_{PLH\,I}$	output signal non-inverted	27		340		ns
	$t_{PLH\,II}$	output signal inverted			340		ns
	$t_{PLH\,III}$	input pin 15			270		ns
Propagation delay	$t_{PHL\,I}$	output signal non-inverted			230		ns
	$t_{PHL\,II}$	output signal inverted			300		ns
	$t_{PHL\,III}$	input pin 15			400		ns
Transition time	t_{TLH}	$C_L = 10\,pF$			330		ns
	t_{THL}				200		ns

Electrical characteristics, 15 V range
Temperature range 1 and 5

Supply voltage	V_S			13.5	15	17	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	15	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$	16			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$, $V_{IL} = 4.5\,V$, $-I_{QH} = 0.1\,mA$	16	12	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5\,V$, $I_{QL} = 30\,mA$	15		1	1.7	V
DC noise margin							
H-signal	V_{nm}			4.5	8		V
L-signal	V_{nm}			2.8	5		V
H-input current at R_1, C_1, R_2, C_2	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	17			2	µA
H-input current remaining inputs	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	17			1	µA
L-input current at R_1, C_1, R_2, C_2	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$	18		1.2	3	mA
L-input current remaining inputs	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$	18		0.6	1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_I = 0\,V$	19	15	37	60	mA
H-supply current	I_S	$V_S = V_{SA}$, $V_I = 0\,V$	20		18	29	mA
L-supply current	I_{SL}	$V_S = V_{SA}$, $V_I = V_{IHA}$	21		12	21	mA
Power consumption	P	$V_S = V_{SA}$, duty cycle 1:1			225	425	mW

Delay times, $V_S = 15\,V$, $F_Q = 1$, $T_{amb} = 25°C$

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Propagation delay	$t_{PLH\ I}$	output signal non-inverted	27		340		ns
	$t_{PLH\ II}$	output signal inverted			280		ns
	$t_{PLH\ III}$	input pin 15			270		ns
Propagation delay	$t_{PHL\ I}$	output signal non-inverted			270		ns
	$t_{PHL\ II}$	output signal inverted			350		ns
	$t_{PHL\ III}$	input pin 15			470		ns
Transition time	t_{TLH}	$C_L = 10\,pF$			350		ns
	t_{THL}				220		ns



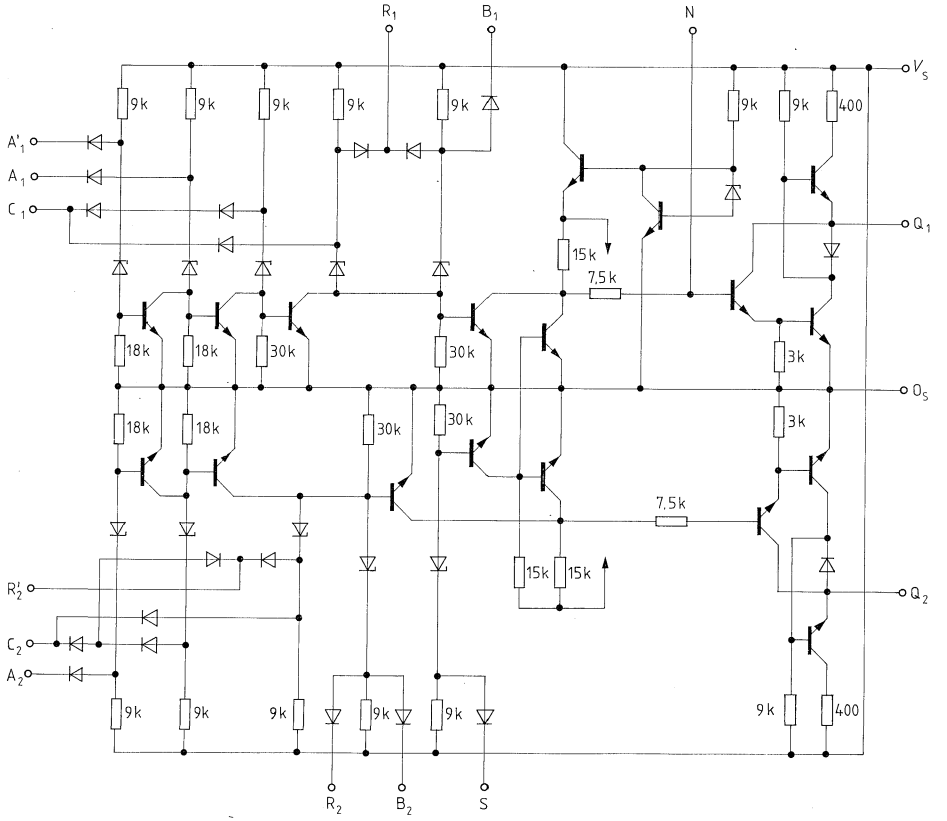
Pin configuration
top view

Logic data, each gate		Upper limit A
H-output load factor	F_{QH}	100
L-output load factor (LSL load)	F_{QL}	16
L-output load factor (FZH 151 as load)	F_{QL}	20
Input load factor at R_1, C_1, R_2, C_2	F_I	2
Input load factor, remaining inputs	F_I	1

Logic function $Q_1 = \overline{S} \vee (A_1 \wedge A_1' \wedge R_1 \wedge C_1) \vee (B_1 \wedge R_1 \wedge \overline{C_1})$

$Q_2 = \overline{S} \vee (A_2 \wedge C_2 \wedge R_2') \vee (B_2 \wedge R_2 \wedge \overline{C_2 \wedge R_2'})$

Schematic


R1
B1
N
Vs
A'1
A1
C1
Q1
Qs
Q2
R'2
C2
A2
R2
B2
S
9k
400
15k
7,5k
18k
30k
3k
7,5k

Type	Ordering code
FZH 161	Q67000-H288
FZH 165 B	Q67000-H289-B

FZH 161 and FZH 165 contain 4 LSL-TTL level converters, each. These can be used as LSL wired AND stages. Calculation of the common collector load resistance is carried out as stated on the following pages.
If wired AND connections and N wiring are used, the capacitance values C_N must all be identical.
The maximum permissible voltage at output Q is 18 V for FZH 161 and 30 V for FZH 165 B; the maximum current being 20 mA.
The permissible input voltage for FZH 165 B is 30 V.

Electrical characteristics, 12 V range
Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	9	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$	10			4.5	V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5$ V, $I_{QL} = 20$ mA	9			0.4	V
DC noise margin							
H-signal	V_{nm}			2.5	5		V
L-signal	V_{nm}			2.8	5		V
H-input current							
at input pins 2, 5, 11, 14	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	11			1	µA
at input pins 1, 15	I_{IH}					2	µA
L-input current							
at input pins 2, 5, 11, 14	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V	12		0.8	1.5	mA
at input pins 1, 15	$-I_{IL}$				1.6	3	mA
H-output current, each output	I_{QH}	$V_S = V_{SA}$, $V_Q = 18$ V/30 V	10			80	µA
H-supply current, each gate	I_{SH}	$V_S = V_{SA}$, $V_I = 0$ V	14		2.5	4.5	mA
L-supply current, each gate	I_{SI}	$V_S = V_{SA}$, $V_I = V_{IHA}$	13		4	6	mA
Power consumption, each gate	P	$V_S = V_{SA}$, duty cycle 1:1			39	70	mW

Delay times, $V_S = 12$ V, $T_{amb} = 25$ °C

Propagation delay	t_{PLH}	$C_L = 15$ pF, $R_C = 760$, $V_{SC} = 12$ V	28	80	250	500	ns
	t_{PHL}			80	130	300	ns
	t_{PLH}	$C_L = 15$ pF, $R_C = 320$, $V_{SC} = 5$ V		80	230	500	ns
	t_{PHL}			80	120	300	ns
Transition time	t_{TLH}	$C_L = 15$ pF, $R_L = 760$, $V_{SC} = 12$ V		50	75	100	ns
	t_{THL}			15	30	50	ns
	t_{TLH}	$C_L = 15$ pF, $R_C = 320$, $V_{SC} = 5$ V		20	45	70	ns
	t_{THL}			6	12	25	ns

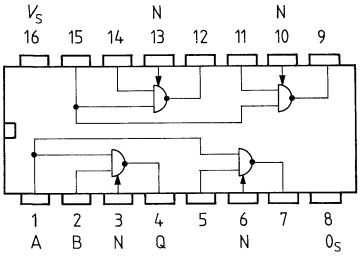
Electrical characteristics, 15 V range

Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			13.5	15	17	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	9	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$	10			4.5	V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5$ V, $I_{QL} = 20$ mA	9			0.4	V
DC noise margin							
H-signal	V_{nm}			4.5	8		V
L-signal	V_{nm}			2.8	5		V
H-input current							
at input pins 2, 5, 11, 14	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	11			1	µA
at input pins 1, 15	I_{IH}					2	µA
L-input current							
at input pins 2, 5, 11, 14	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V	12		1	1.8	mA
at input pins 1, 15	$-I_{IL}$				2	3.6	mA
H-output current, each output	I_{QH}	$V_S = V_{SA}$, $V_Q = 18$ V/30 V	10			80	µA
H-supply current, each gate	I_{SH}	$V_S = V_{SA}$, $V_I = 0$ V	14		2.8	4.5	mA
L-supply current, each gate	I_{SL}	$V_S = V_{SA}$, $V_I = V_{IHA}$	13		4.5	7	mA
Power consumption, each gate	P	$V_S = V_{SA}$, duty cycle 1:1			55	78	mW

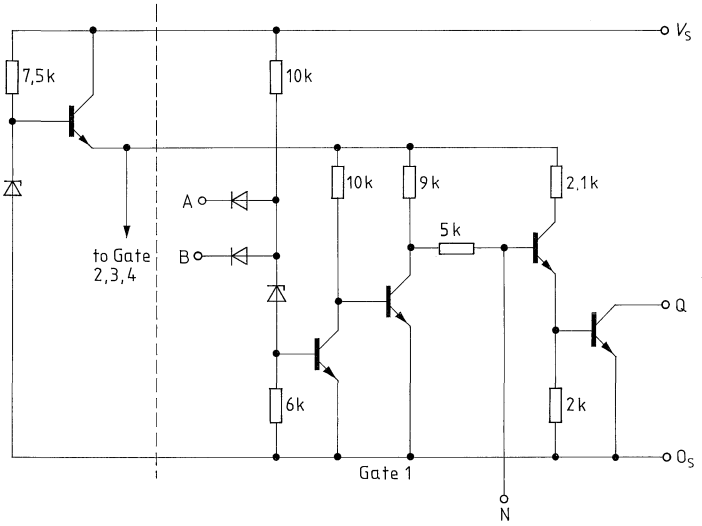
Delay times, $V_S = 15$ V, $T_{amb} = 25$ °C

Propagation delay	t_{PLH}	$C_L = 15$ pF, $R_C = 760$, $V_{SC} = 15$ V	28		180	ns
	t_{PHL}				140	ns
	t_{PLH}	$C_L = 15$ pF, $R_C = 320$, $V_{SC} = 5$ V			270	ns
	t_{PHL}				120	ns
Transition time	t_{TLH}	$C_L = 15$ pF, $R_L = 760$, $V_{SC} = 15$ V			70	ns
	t_{THL}				30	ns
	t_{TLH}	$C_L = 15$ pF, $R_C = 320$, $V_{SC} = 5$ V			35	ns
	t_{THL}				11	ns



Pin configuration
top view

Schematic (one gate)



Logic data, each gate		Upper limit A
L-output load factor	F_{QL}	10
Input load factor, input A	F_I	2
Input load factor, input B	F_I	1
Logic function	$Q = \overline{A \wedge B}$	

Calculation of the collector load resistance R_C

The resistance R_C is calculated from the necessary voltage variations and the input and output currents as follows:

$$R_{CA} = \frac{V_{SC} - V_{QH}\ \text{V}}{nI_{QH} + NI_{IH}\ \mu\text{A}}$$

$$R_{CB} = \frac{V_{SC} - V_{QL}\ \text{V}}{I_{QL} - NI_{IL}\ \text{mA}}$$

where: V_{SC} = supply voltage of the load resistor
n = number of AND connections
N = number of inputs connected

The resistance used in the circuit must lie between the upper and lower limits A and B.

For use as a **level converter**, the following values result:

FZH 161/165 B, LSL TTL:

$$R_{CA} = \frac{5 - 2.4\ \text{V}}{n\,80 + N\,40\ \mu\text{A}} \qquad R_{CB} = \frac{5 - 0.4\ \text{V}}{20 - N\,1.6\ \text{mA}}$$

where: $n_A = 2$ for $N_A = 10$

FZH 181/185, TTL $LSL_{12\,V}$:

$$R_{CA} = \frac{12 - 10\ \text{V}}{n\,250 + N\,1\ \mu\text{A}} \qquad R_{CB} = \frac{12 - 1\ \text{V}}{50 - N\,1.5\ \text{mA}}$$

TTL $LSL_{15\,V}$:

$$R_{CA} = \frac{15 - 12\ \text{V}}{n\,250 + N\,1\ \mu\text{A}} \qquad R_{CB} = \frac{15 - 1\ \text{V}}{50 - N\,1.8\ \text{mA}}$$

where: $n_A = 4$ for $N_A = 25$

If FZH 165 and FZH 165 B are used for **wired AND connections**, then the following values result:

in the 12 V range:

$$R_{CA} = \frac{12 - 10\ \text{V}}{n\,80 + N\,1\ \mu\text{A}} \qquad R_{CB} = \frac{12 - 0.4\ \text{V}}{20 - N\,1.5\ \text{mA}}$$

and in the 15 V range:

$$R_{CA} = \frac{15 - 12\ \text{V}}{n\,80 + N\,1\ \mu\text{A}} \qquad R_{CB} = \frac{12 - 0.4\ \text{V}}{20 - N\,1.8\ \text{mA}}$$

where: $n_A = 9$ for $N_A = 10$

Type	Ordering code
FZH 181	Q67000-H326
FZH 185	Q67000-H327

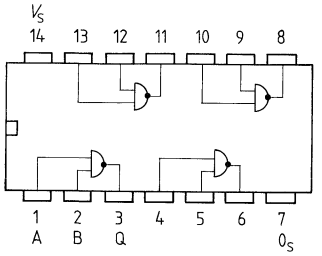
FZH 181 and FZH 185 contain four TTL-LSL level converters, each, which can also be used in wired AND connections. The formulae shown on the previous page are used for calculation of the common collector load resistance. The maximum permissible voltage at output Q is 18 V, and the maximum current 50 mA.

Electrical characteristics
Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			4.75	5	5.25	V
H-input voltage	V_{IH}	$V_S = 4.75\,V$	1	2			V
L-input voltage	V_{IL}	$V_S = 4.75\,V$	8			0.8	V
H-output current	I_{QH}	$V_S = 4.75\,V$, $V_{IL} = 0.8\,V$, $V_{QH} = 18\,V$	8			250	µA
L-output voltage	V_{QL}	$V_S = 4.75\,V$, $V_{IH} = 2.0\,V$, $I_{QL} = 16\,mA$	1			0.4	V
	V_{QL}	$V_S = 4.75\,V$, $V_{IH} = 2.0\,V$ $I_{QL} = 50\,mA$	1			1	V
DC noise margin	V_{nm}			0.4	1		V
Input current each input	I_I	$V_S = 5.25\,V$, $V_I = 5.5\,V$	3			1	mA
H-input current each input	I_{IH}	$V_S = 5.25\,V$, $V_{IH} = 2.4\,V$	3			80	µA
L-input current each input	$-I_{IL}$	$V_S = 5.25\,V$, $V_{IL} = 0.4\,V$	4			1.6	mA
H-supply current, each gate	I_{SH}	$V_S = 5\,V$, $V_I = 0\,V$	6		1	2	mA
L-supply current, each gate	I_{SL}	$V_S = 5\,V$, $V_I = 5\,V$	7		8.5	12	mA
Power consumption, each gate	P	$V_S = V_{SA}$, duty cycle 1:1			24	37	mW

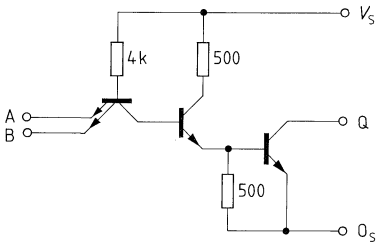
Delay times, $V_S = 5\,V$, $T_{amb} = 25\,^{\circ}C$

Propagation delay	t_{PLH}	$C_L = 15\,pF$, $R_C = 760\,\Omega$, $V_{SC} = 12\,V$	29		130	300	ns
	t_{PHL}				20	60	ns



Pin configuration
top view

Schematic (one gate)



Logic data, each gate		Upper limit A
L-output load factor	F_{QL}	10
Input load factor, each input (TTL load)	F_I	1
Logic function	$Q = \overline{A \wedge B}$	

Type	Ordering code
FZH 101 A	Q67000-H1242
FZH 105 A	Q67000-H1241
FZH 111 A	Q67000-H191
FZH 115 B	Q67000-H215-B
FZH 191	Q67000-H633
FZH 195	Q67000-H634
FZH 201	Q67000-H636
FZH 205	Q67000-H637

FZH 101 A, FZH 105 A: Quad 2-input NAND gate
FZH 111 A, FZH 115 B: Quad 2-input NAND gate with N-input
FZH 191, FZH 195: Triple 3-input NAND gate with N-input
FZH 201, FZH 205: Hex inverter with strobe inputs
The permissible input voltage of the FZH 115 B is 30 V.

Electrical characteristics, 12 V range
Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}	2			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA}, $V_{IL} = 4.5\,V$, $-I_{QH} = 0.1\,mA$	2	10	11.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5\,V$, $I_{QL} = 15\,mA$	1		0.9	1.7	V
DC noise margin							
H-signal	V_{nm}			2.5	5		V
L-signal	V_{nm}			2.8	5		V
H-input current, each input	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	3			1	µA
at strobe 1	I_{IH}					4	µA
at strobe 2	I_{IH}					2	µA
L-input current, each input	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$	4		0.8	1.5	mA
at strobe 1	I_{IL}					6	mA
at strobe 2	I_{IL}					3	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_Q = 0\,V$	5	9	15	25	mA
H-supply current, each gate	I_{SH}	$V_S = V_{SA}$, $V_I = 0\,V$	6		0.9	1.6	mA
L-supply current, each gate	I_{SL}	$V_S = V_{SA}$, $V_I = V_{IHA}$	7		1.7	3	mA
Power consumption, each gate	P	$V_S = V_{SA}$ duty cycle 1:1			15	31	mW

The FZH 101 A/105 A and FZH 111 A/115 B with short-circuit protection replace the FZH 101/105 and FZH 111/115 without short-circuit protection.

Delay times, $V_S = 12\,V$, $F_Q = 1$, $T_{amb} = 25°\,C$

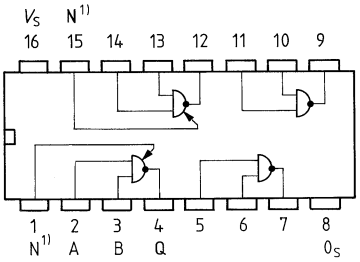
		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Propagation delay	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	26	90	175	310	ns
	t_{PHL}			90	175	310	ns
Transition time	t_{TLH}	$C_L = 10\,pF$		200	340	570	ns
	t_{THL}			70	120	210	ns

Electrical characteristics, 15 V range
Temperature range 1 and 5

Supply voltage	V_S			13.5	15	17	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}	2			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA}, $V_{IL} = 4.5\,V$, $-I_{QH} = 0.1\,mA$	2	12	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5\,V$, $I_{QL} = 18\,mA$	1		1	1.7	V
DC noise margin							
H-signal	V_{nm}			4.5	8		V
L-signal	V_{nm}			2.8	5		V
H-input current							
each input	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	3			1	µA
at strobe 1	I_{IH}					4	µA
at strobe 2	I_{IH}					2	µA
L-input current							
each input	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$	4		1	1.8	mA
at strobe 1	I_{IL}					7.2	mA
at strobe 2	I_{IL}					3.6	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_Q = 0\,V$	5	9	15	25	mA
H-supply current, each gate	I_{SH}	$V_S = V_{SA}$, $V_I = 0\,V$	6		1.2	2.1	mA
L-supply current, each gate	I_{SL}	$V_S = V_{SA}$, $V_I = V_{IHA}$	7		2.3	4	mA
Power consumption, each gate	P	$V_S = V_{SA}$, duty cycle 1:1			27	51	mW

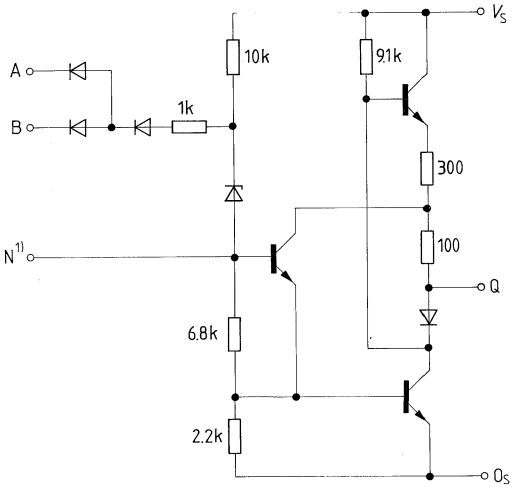
Delay times, $V_S = 15\,V$, $F_Q = 1$, $T_{amb} = 25°\,C$

Propagation delay	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	26		195		ns
	t_{PHL}				140		ns
Transition time	t_{TLH}	$C_L = 10\,pF$			410		ns
	t_{THL}				75		ns



Pin configuration
top view

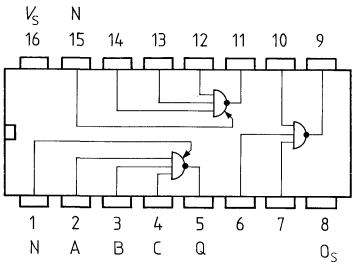
Schematic (one gate)



Logic data, each gate		Upper limit A
H-output load factor	F_{QH}	100
L-output load factor	F_{QL}	10
Input load factor, each input	F_I	1

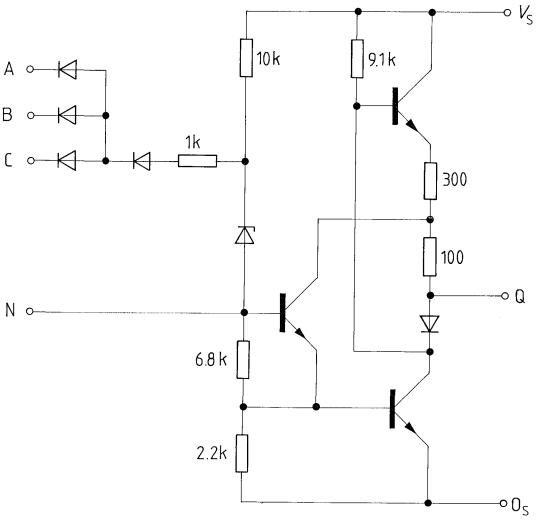
Logic function $Q = \overline{A \wedge B}$

[1)] FZH 111 A/115 B only



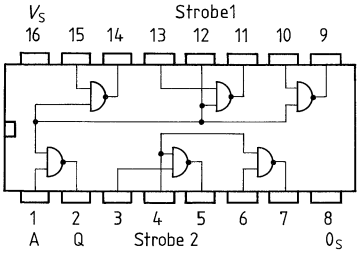
Pin configuration
top view

Schematic (one gate)



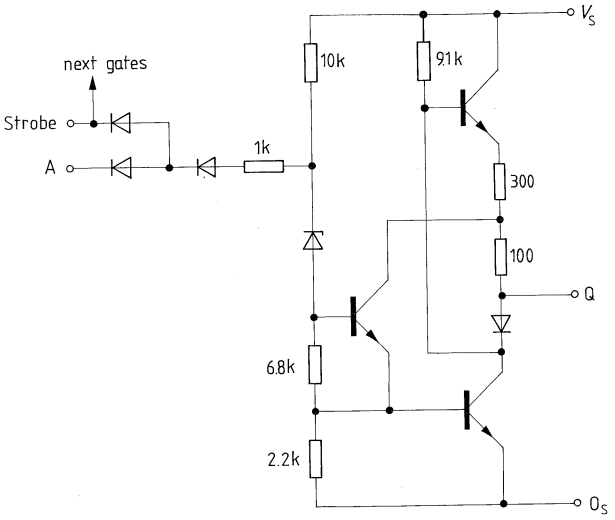
Logic data, each gate		Upper limit A
H-output load factor	F_{QH}	100
L-output load factor	F_{QL}	10
Input load factor, each input	F_I	1

Logic function $Q = \overline{A \wedge B \wedge C}$



Pin configuration
top view

Schematic (one gate)



Logic data, each gate			Upper limit A
H-output load factor		F_{QH}	100
L-output load factor		F_{QL}	10
Input load factor	A-inputs	F_I	1
	strobe 1	F_I	4
	strobe 2	F_I	2

Logic function $Q = \overline{A \wedge \text{Strobe}}$

Type	Ordering code
FZH 211	Q67000-H639
FZH 215 B	Q67000-H640-B
FZH 231	Q67000-H642
FZH 235	Q67000-H643

FZH 211, FZH 215 B: Quad 2-input NAND gate with open collector output and N-input
FZH 231, FZH 235: Dual 5-input NAND gate with open collector output and N-input

Calculation of the collector resistors for wired AND connection is carried out as described for FZH 161/181. In the case of wired AND connection and N wiring, the capacitors C_N must have equal values.

The maximum permissible voltage at the outputs is 18 V (30 V for FZH 215 B) and the maximum current 18 mA. The maximum permissible input voltage of the FZH 215 B is 30 V.

Electrical characteristics, 12 V range
Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}	2			4.5	V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5$ V, $I_{QL} = 15$ mA	1		0.9	1.7	V
DC noise margin							
H-signal	V_{nm}			2.5	5		V
L-signal	V_{nm}			2.8	5		V
H-input current, each input	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	3			1	µA
L-input current, each input	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V	4		0.8	1.5	mA
H-output current	I_{QH}	$V_S = V_{SB}$, $V_{IL} = 4.5$ V, $V_{QH} = 18$ V or 30 V	8			80	µA
H-supply current, each gate	I_{SH}	$V_S = V_{SA}$, $V_I = 0$ V	6		1	1.7	mA
L-supply current, each gate	I_{SL}	$V_S = V_{SA}$, $V_I = V_{IHA}$	7		0.4	1	mA
Power consumption, each gate	P	$V_S = V_{SA}$ duty cycle 1:1			8.5	18	mW

Delay times, $V_S = 12$ V, $T_{amb} = 25°$ C

Propagation delay	t_{PLH}	$V_{SC} = 12$ V, $C_L = 15$ pF, $R_C = 760\,\Omega$	28	30	70	150	ns
	t_{PHL}			90	175	310	ns
Transition time	t_{TLH}			120	230	450	ns
	t_{THL}			70	120	210	ns

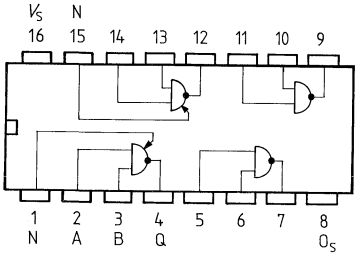
Electrical characteristics, 15 V range

Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			13.5	15	17	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}	2			4.5	V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5$ V, $I_{QL} = 18$ mA	1		1	1.7	V
DC noise margin							
H-signal	V_{nm}			4.5	8		V
L-signal	V_{nm}			2.8	5		V
H-input current each input	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	3			1	µA
L-input current, each input	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V	4		1	1.8	mA
H-output current, each output	I_{QH}	$V_S = V_{SB}$, $V_{IL} = 4.5$ V, $V_{QH} = 18$ V or 30 V	8			80	µA
H-supply current each gate	I_{SH}	$V_S = V_{SA}$, $V_I = 0$ V	6		1.3	2.1	mA
L-supply current, each gate	I_{SL}	$V_S = V_{SA}$, $V_I = V_{IHA}$	7		0.7	1.4	mA
Power consumption each gate	P	$V_S = V_{SA}$ duty cycle 1:1			15	30	mW

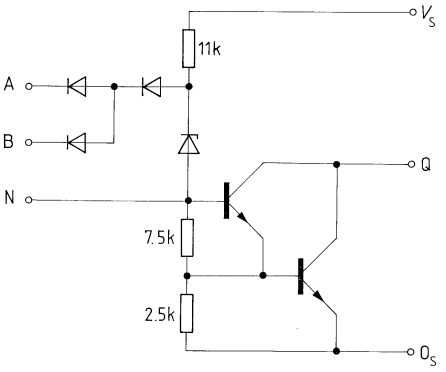
Delay times, $V_S = 15$ V, $T_{amb} = 25°$ C

Propagation delay	t_{PLH}	$V_{SC} = 15$ V, $C_L = 15$ pF, $R_C = 760\,\Omega$	28		90		ns
	t_{PHL}				155		ns
Transition time	t_{TLH}				300		ns
	t_{THL}				70		ns

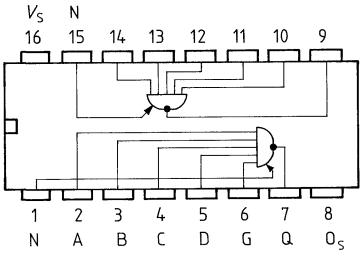


Pin configuration
top view

Schematic (one gate)

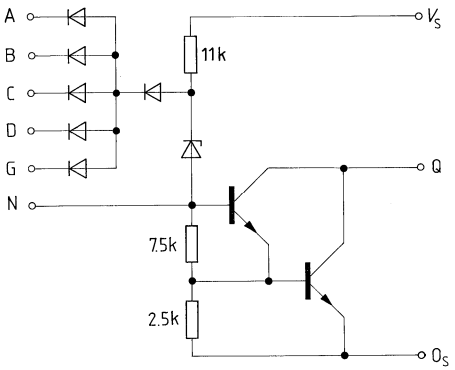


Logic data, each gate		Upper limit A
L-output load factor	F_{QL}	10
Input load factor, each input	F_I	1
Logic function	$Q = \overline{A \wedge B}$	



Pin configuration
top view

Schematic (one gate)



Logic data, each gate		Upper limit A
L-output load factor	F_{QL}	10
Input load factor, each input	F_I	1

Logic function $Q = \overline{A \wedge B \wedge C \wedge D \wedge G}$

Preliminary data

Type	Ordering code
FZH 211 S	Q67000-H639-S1

Four NAND drivers with open collector outputs, 2 inputs, and N inputs for delay circuits. The input threshold can be switched to LSL, TTL, or CMOS level, depending on the supply voltage used.

Main application

Driver up to 30 V/150 mA, relay driver, and level converter.

Calculation of the load resistance for wired AND connection is carried out as described for FZH 161/181. In the case of wired AND connection and N wiring, the capacitors C_N must have identical values.

Additional maximum ratings

		Test conditions	Lower limit B	Upper limit A	Unit
Supply voltage	V_S		0	30	V
Input voltage	V_I		−0.5	30	V
Voltage between 2 inputs	V_{II}			30	V
Voltage at output, output transistor cut off	$V_{QH\ sust}$			30	V
Voltage at output, output transistor conducting	V_{QL}		0		V
Output current	I_{QL}			150	mA
Capacitance at Q	C_L			5	nF
Capacitance between N and Q	C_N			0.1	µF

Otherwise, the maximum ratings defined for the LSL series FZ 100 apply.

Functional range

Temperature range 1

Supply voltage range 1	V_S	TTL threshold at A, B	4	7	V
Supply voltage range 2	V_S	LSL threshold at A, B	9	30	V
Supply voltage	V_S	Switching of threshold at A, B at V_S = 8 V, typical	4	30	V

Electrical characteristics in the 5 V range

Temperature range 1

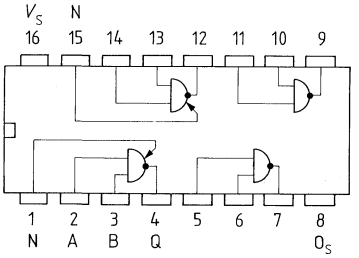
		Test conditions	Test circuit[2])	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			4		7	V
H-input voltage	V_{IH}	L at Q	3	2			V
L-input voltage	V_{IL}	H at Q	2			0.8	V
L-output voltage	V_{QL}	$V_{IH} = 2\,V$, $I_{QL} = 1.6\,mA$	4		0.7	0.8	V
L-output voltage	V_{QL}	$V_{IH} = 2\,V$, $I_{QL} = 100\,mA$	4			1.3	V
L-output voltage[1])	V_{QL}	$V_{IH} = 2\,V$, $I_{QL} = 150\,mA$	4			1.5	V
H-input current	I_{IH}	$V_{IH} = 30\,V$	3			1	µA
L-input current	$-I_{IL}$	$V_{IL} = 0\,V$	2		5	50	µA
H-output current	I_{QL}	$V_{IL} = 0.8\,V$, $V_{QH} = 30\,V$	5			50	µA
Input current per package	I_S	$V_S = 7\,V$	1	1.5	3	4	mA

Electrical characteristics in the 12 V, 15 V, 24 V ranges

Temperature range 1

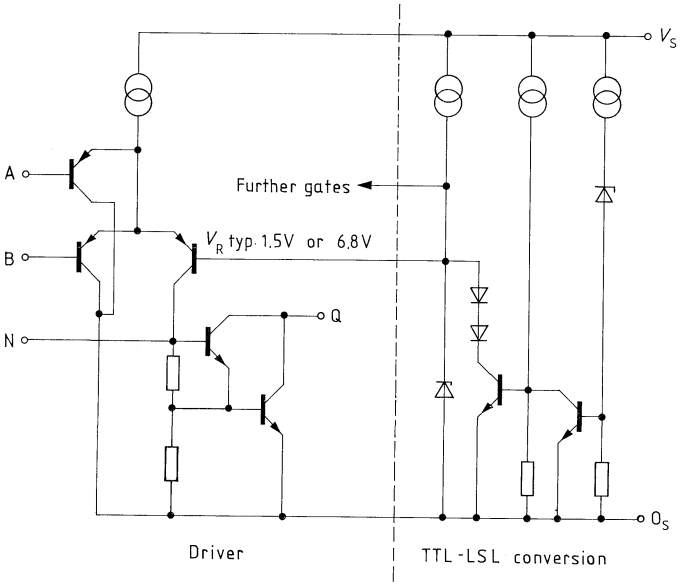
Supply voltage	$SK2V_S$			9		30	V
H-input voltage	V_{IH}	L at Q	3	8			V
L-input voltage	V_{IL}	H at Q	2			6	V
L-output voltage	V_{QL}	$V_{IH} = 8\,V$, $I_{QL} - 100\,mA$	4		1	1.3	V
L-output voltage[1])	V_{QL}	$V_{IH} = 8\,V$, $I_{QL} = 150\,mA$	4			1.5	V
H-input current	I_{IH}	$V_{IH} = 30\,V$	3			1	µA
L-input current	$-I_{IL}$	$V_{IL} = 0\,V$	2		5	50	µA
H-output current	I_{QH}	$V_{IL} = 6\,V$, $V_{QH} = 30\,V$	5			50	µA
Input current per package	I_S	$V_S = 30\,V$	1	1.5	3	4	mA

[1]) The sum of all output currents per package must not exceed 400 mA.
[2]) The test circuits described for the LSL series FZ 100 are used, but with open collectors.



Pin configuration
top view

Schematic (one gate)



Logic function $Q = \overline{A \wedge B}$

Type	Ordering code
FZH 241	Q67000-H645
FZH 245 B	Q67000-H646-B

The NAND Schmitt triggers can be expanded as required with the aid of BAW 76 diodes, whose anodes must be connected in parallel to the expander input N_1.
If the power supply is unregulated, a decoupling capacitor of 1 µF should be connected directly to pin 16. The maximum permissible input voltage of FZH 245 B is 30 V.

Electrical characteristics, 12 V range

Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			11.4	12	13.5	V
Upper threshold voltage	V_{Tu}	$V_S = 12.0\,V$	2	5.5	6.5	7.5	V
Lower threshold voltage	V_{Tl}	$V_S = 12.0\,V$	2	5	5.6	7	V
Hysteresis	V_{HY}	$V_S = 12.0\,V$	2	0.5	0.9	1.3	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA}, $V_{IL} = 4.5\,V$, $-I_{QH} = 0.1\,mA$	2	10	11.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5\,V$, $I_{QL} = 15\,mA$	1		0.9	1.7	V
DC noise margin							
H-signal	V_{nm}			2.5	5		V
L-signal	V_{nm}			2.8	5		V
H-input current, each input	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	3			1	µA
L-input current, each input	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$	4			1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_I = 0\,V$	5	9	15	25	mA
H-supply current, each gate	I_{SH}	$V_S = V_{SA}$, $V_I = 0\,V$	6		4	6.3	mA
L-supply current, each gate	I_{SL}	$V_S = V_{SA}$, $V_I = V_{IHA}$	7		4	6.3	mA

Delay times, $V_S = 12\,V$, $F_Q = 1$, $T_{amb} = 25°C$

Propagation delay	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	26	90	175	310	ns
	t_{PHL}			90	175	310	ns
Transition time	t_{TLH}	$C_L = 10\,pF$		200	340	570	ns
	t_{THL}			70	120	210	ns

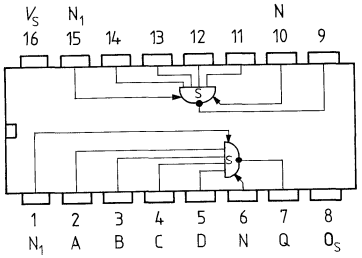
Electrical characteristics, 15 V range

Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			13.5	15	17	V
Upper threshold voltage	V_{Tu}	$V_S = 15.0\,V$	2	5.4	6.4	7.4	V
Lower threshold voltage	V_{Tl}	$V_S = 15.0\,V$	2	6.9	5.5	4.9	V
Hysteresis	V_{HY}	$V_S = 15.0\,V$	2	0.5	0.9	1.3	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA}, $V_{IL} = 4.5\,V$, $-I_{QH} = 0.1\,mA$	2	12	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5\,V$, $I_{QL} = 18\,mA$	1		1.1	1.7	V
DC noise margin							
H-signal	V_{nm}			4.5	8		V
L-signal	V_{nm}			2.8	5		V
H-input current, each input	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	3			1	µA
L-input current, each input	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$	4			1.8	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_I = 0\,V$	5	9	15	25	mA
H-supply current, each gate	I_{SH}	$V_S = V_{SA}$, $V_I = 0\,V$	6		4.5	7.3	mA
L-supply current, each gate	I_{SL}	$V_S = V_{SA}$, $V_I = V_{IHA}$	7		5	8	mA

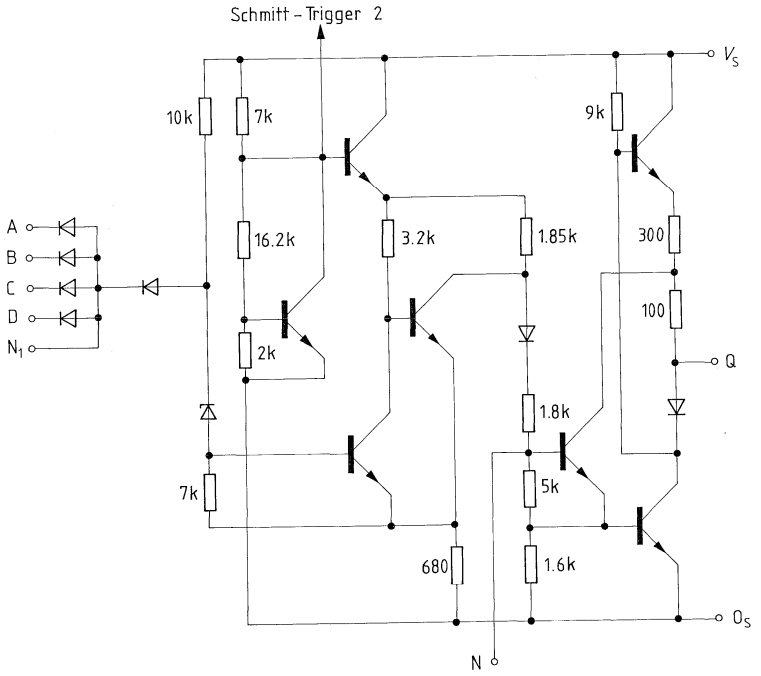
Delay times, $V_S = 15\,V$, $F_Q = 1$, $T_{amb} = 25°C$

Propagation delay	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	26		205		ns
	t_{PHL}				170		ns
Transition time	t_{TLH}	$C_L = 10\,pF$			340		ns
	t_{THL}				120		ns



Pin configuration
top view

Schematic (one gate)



Logic data, each gate		Upper limit A
H-output load factor	F_{OH}	100
L-output load factor	F_{OL}	10
Input load factor, each input	F_I	1

Logic function $Q = \overline{A \wedge B \wedge C \wedge D}$

Type	Ordering code
FZH 251	Q67000-H817
FZH 255 B	Q67000-H818-B
FZH 261	Q67000-H819
FZH 265 B	Q67000-H820-B
FZH 271	Q67000-H821
FZH 275	Q67000-H822
FZH 281	Q67000-H823
FZH 285 B	Q67000-H824-B
FZH 291	Q67000-H825
FZH 295 B	Q67000-H826-B

FZH 251/255 B: Quad 2-input AND gate with N-input
FZH 261/265 B: Dual 2-input NAND gate and quad inverter
FZH 271/275: Quad 2-input exclusive-OR gate with N-input
FZH 281/285 B: Quad 2-input NOR gate with N-input
FZH 291/295 B: Quad 2-input OR gate with N-input
The maximum permissible input of the B types is 30 V.

Electrical characteristics, 12 V range
Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ and V_{SB}	2			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA}, $-I_{QH} = 0.1$ mA	2	10	11.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $I_{QL} = 15$ mA	1		0.9	1.7	V
DC noise margin							
H-signal	V_{nm}			2.5	5		V
L-signal	V_{nm}			2.8	5		V
H-input current each input	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	3			1	µA
L-input current each input	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V	4		0.8	1.5	mA
Short-circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_Q = 0$ V	5	9	15	25	mA

Electrical characteristics, 12 V range

Temperature range 1 and 5

		Test conditions		Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply currents								
FZH 251/255 B								
H-supply current	I_{SH}	$V_I = V_{IHA}$	$V_S = V_{SA}$	6		6.4	12.5	mA
L-supply current	I_{SL}	$V_I = 0\,V$		7		9.6	18	mA
FZH 261/265 B								
H-supply current	I_{SH}	$V_I = 0\,V$	$V_S = V_{SA}$	6		6.2	12.5	mA
L-supply current	I_{SL}	$V_I = V_{IHA}$		7		10.2	18	mA
FZH 271/275								
H-supply current	I_{SH}	$V_{I1} = V_{IHA}$, $V_{I2} = 0\,V$	$V_S = V_{SA}$	6		13.8	21.5	mA
L-supply current	I_{SL}	$V_I = 0\,V$		7		15.2	24	mA
FZH 281/285 B								
H-supply current	I_{SH}	$V_I = 0\,V$	$V_S = V_{SA}$	6		13.2	21.5	mA
L-supply current	I_{SL}	$V_I = V_{IHA}$		7		14.8	24	mA
FZH 291/295 B								
H-supply current	I_{SH}	$V_I = V_{IHA}$	$V_S = V_{SA}$	6		9	14	mA
L-supply current	I_{SL}	$V_I = 0\,V$		7		14.4	24	mA

Electrical characteristics, 15 V range

Temperature range 1 and 5

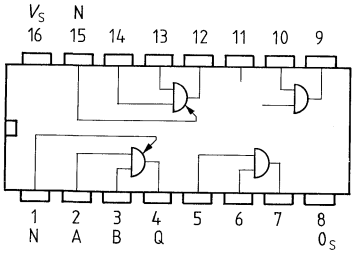
		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			13.5	15	17	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}	2			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA}, $-I_{QH} = 0.1$ mA	2	12	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $I_{QL} = 18$ mA	1		1	1.7	V
DC noise margin							
H-signal	V_{nm}			4.6	8		V
L-signal	V_{nm}			2.8	5		V
H-input current each input	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	3			1	µA
L-input current each input	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V	4		1	1.8	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_Q = 0$ V	5	9	15	25	mA
Supply currents							
FZH 251/255 B							
H-supply current	I_{SH}	$V_I = V_{IHA}$ | $V_S = V_{SA}$	6		8.7	15.5	mA
L-supply current	I_{SL}	$V_I = 0$ V | $V_S = V_{SA}$	7		13.8	24	mA
FZH 261/265 B							
H-supply current	I_{SH}	$V_I = 0$ V | $V_S = V_{SA}$	6		8.2	14.5	mA
L-supply current	I_{SL}	$V_I = V_{IHA}$ | $V_S = V_{SA}$	7		14.4	24	mA
FZH 271/275							
H-supply current	I_{SH}	$V_{I1} = V_{IHA}$, $V_{I2} = 0$ V | $V_S = V_{SA}$	6		16.4	24	mA
L-supply current	I_{SL}	$V_I = 0$ V | $V_S = V_{SA}$	7		19.2	30	mA
FZH 281/285 B							
H-supply current	I_{SH}	$V_I = 0$ V | $V_S = V_{SA}$	6		15.1	24	mA
L-supply current	I_{SL}	$V_I = V_{IHA}$ | $V_S = V_{SA}$	7		18.8	30	mA
FZH 291/295 B							
H-supply current	I_{SH}	$V_I = V_{IHA}$ | $V_S = V_{SA}$	6		10.5	18.5	mA
L-supply current	I_{SL}	$V_I = 0$ V | $V_S = V_{SA}$	7		18.4	30	mA

Delay times, $V_S = 12\,V$, $F_Q = 1$, $T_{amb} = 25°C$ $\quad Q = A \wedge B$

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
FZH 261/265 B							
Propagation delay	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	26	90	175	310	ns
	t_{PHL}			90	175	310	ns
Transition time	t_{TLH}	$C_L = 10\,pF$		200	340	570	ns
	t_{THL}			70	120	210	ns
FZH 251/255 B, FZH 271/275, FZH 291/295 B							
Propagation delay	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	26	200	340	570	ns
	t_{PHL}			90	175	310	ns
Transition time	t_{TLH}	$C_L = 10\,pF$		200	340	570	ns
	t_{THL}			70	120	210	ns
FZH 281/285 B							
Propagation delay	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	26	90	175	310	ns
	t_{PHL}			200	340	570	ns
Transition time	t_{TLH}	$C_L = 10\,pF$		200	340	570	ns
	t_{THL}			70	120	210	ns

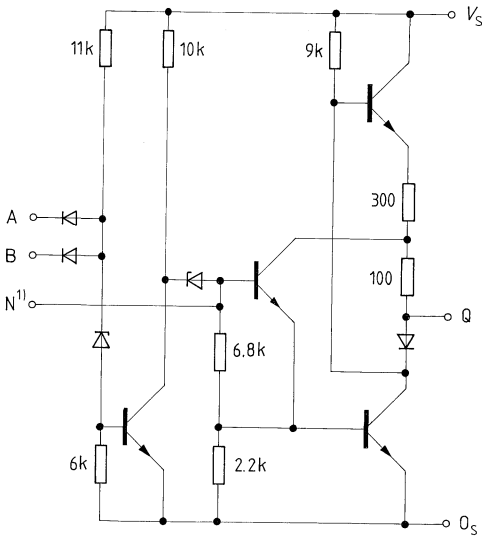
Delay times, $V_S = 15\,V$, $F_Q = 1$, $T_{amb} = 25°C$

FZH 261/265 B							
Propagation delay	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	26		185		ns
	t_{PHL}				150		ns
Transition time	t_{TLH}	$C_L = 10\,pF$			410		ns
	t_{THL}				70		ns
FZH 251/255 B, FZH 271/275, FZH 291/295 B							
Propagation delay	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	26		340		ns
	t_{PHL}				180		ns
Transition time	t_{TLH}	$C_L = 10\,pF$			390		ns
	t_{THL}				130		ns
FZH 281/285 B							
Propagation delay	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	26		305		ns
	t_{PHL}				280		ns
Transition time	t_{TLH}	$C_L = 10\,pF$			340		ns
	t_{THL}				120		ns



Pin configuration
top view

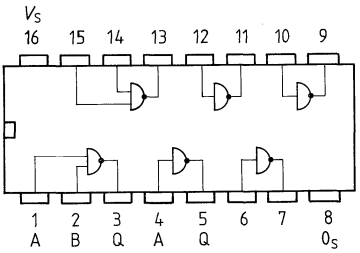
Schematic (one gate)



Logic data, each gate		Upper limit A
H-output load factor	F_{QH}	100
L-output load factor	F_{QL}	10
Input load factor, each input	F_I	1

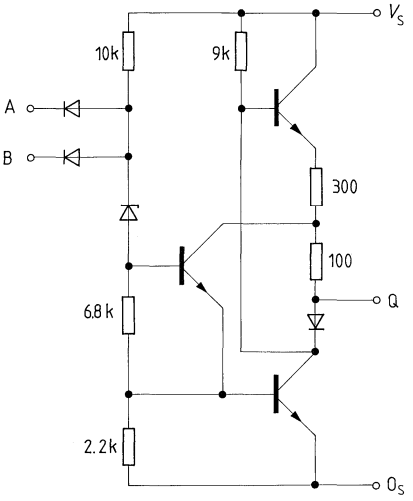
Logic function $Q = A \wedge B$

[1]) Gates 1 and 4 only.



Pin configuration
top view

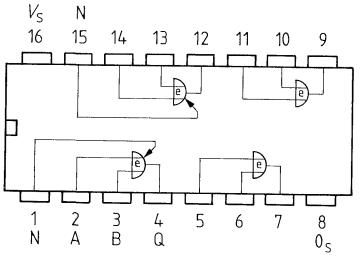
Schematic (one gate)



B-input only on gates 1 and 6

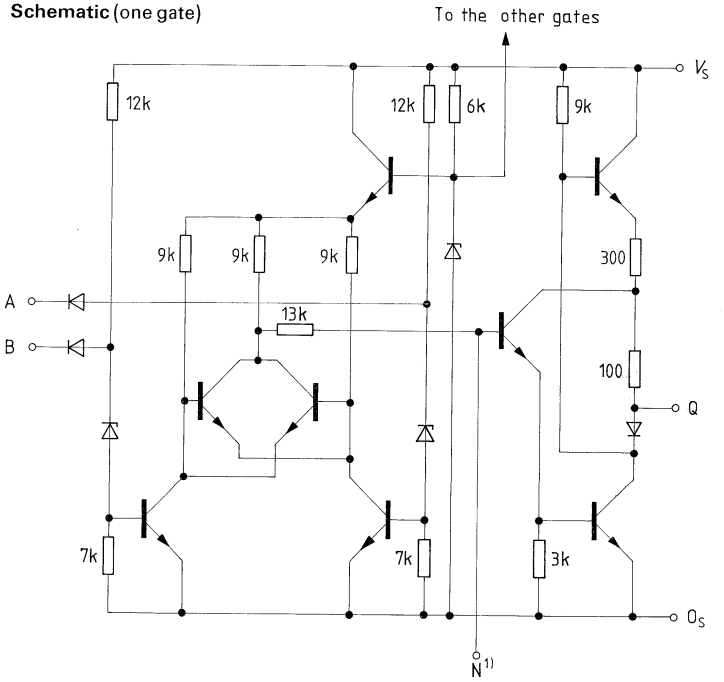
Logic data, each gate		Upper limit A
H-output load factor	F_{QH}	100
L-output load factor	F_{QL}	10
Input load factor, each input	F_I	1

Logic function gates 1 and 6 $Q = \overline{A \wedge B}$
gates 2, 3, 4, and 5 $Q = \overline{A}$



Pin configuration
top view

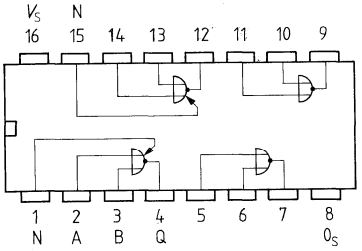
Schematic (one gate)



Logic data, each gate		Upper limit A
H-output load factor	F_{QH}	100
L-output load factor	F_{QL}	10
Input load factor, each input	F_I	1

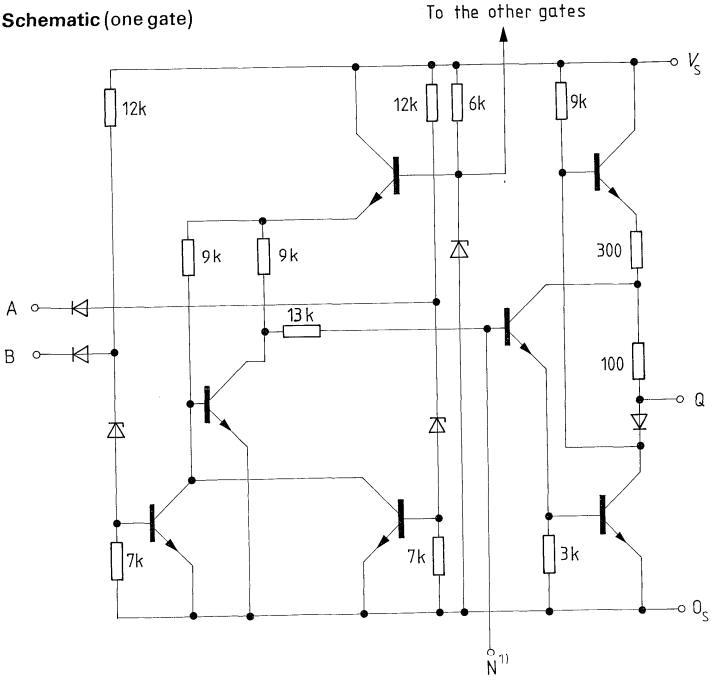
Logic function $Q = (A \wedge \overline{B}) \vee (\overline{A} \wedge B)$

1) Gates 1 and 4 only.



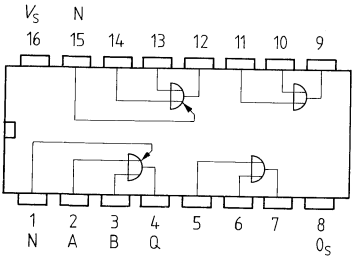
Pin configuration
top view

Schematic (one gate)



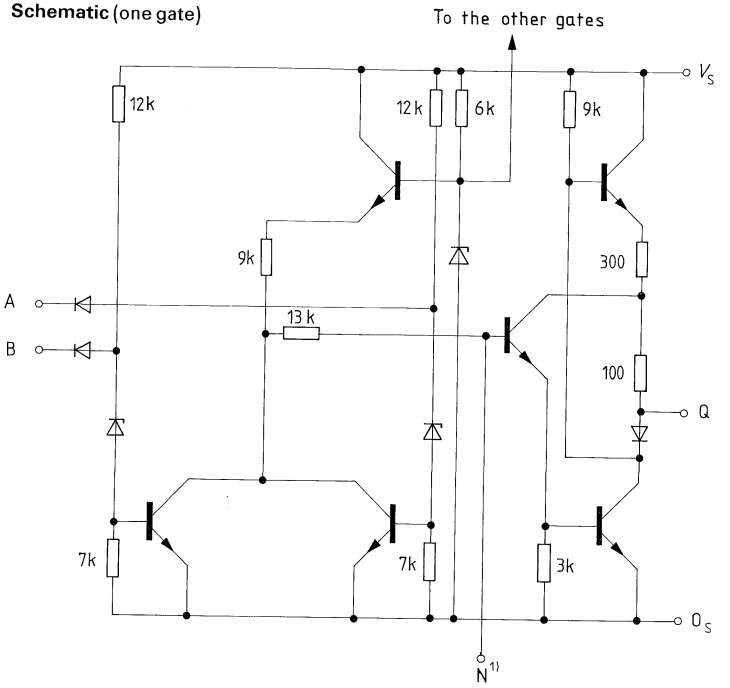
Logic data, each gate		Upper limit A
H-output load factor	F_{QH}	100
L-output load factor	F_{QL}	10
Input load factor, each input	F_I	1
Logic function	$Q = \overline{A \vee B}$	

1) Gates 1 and 4 only.



Pin configuration
top view

Schematic (one gate)



Logic data, each gate		Upper limit A
H-output load factor	F_{QH}	100
L-output load factor,	F_{QL}	10
Input load factor, each input	F_I	1
Logic function		$Q = A \vee B$

[1]) Gates 1 and 4 only.

Quad 2-Input NOR Gate with Destruction Protection

FZH 301
FZH 305

Preliminary data

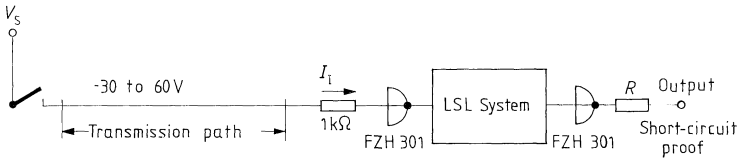
Type	Ordering code
FHZ 301	Q67000–H1586
FHZ 305	Q67000–H1587

The FZH 301 and FZH 305 have the following characteristics: Input voltages up to 30 V; active inputs, i.e. open circuit inputs act as L-signals; destruction protection at inputs and outputs; outputs proof against short circuits to ground and to supply voltage.

Application example

The use of the FZH 301/305 in an electronic control provides protection against overload, short circuit, and wire breakage, both at the inputs and outputs of a system.

The input of the FZH 301/305 is current-controlled, i.e. the circuit functions only when a positive input signal also causes a corresponding input current I_I to flow. This provides protection against wire breakage in the transmission line. Positive signals are necessary to drive the signal, which means that short circuits to ground on the transmission path prevent the circuit from operating. The circuit also contains integrated protective diodes which, with the aid of a series resistor of 1 kΩ, provide effective protection of the inputs in the range −30 to 60 V. The low input current of the circuit also permits the use of higher resistance values. The protective diodes normally connected to such circuits may be omitted.



The output stage of the FZH 301/305 is designed so that short circuits to either ground or to the positive supply voltage are permissible, regardless of the logic state of the output. Integrated protective diodes with a permissible current of ± 30 mA for 30 µs provide protection against overload. If necessary, a series resistor can be fitted to limit the current; the corresponding reduction in the output load factor must be taken into account if this is done. The protective diodes normally connected to such circuits can be omitted.

Additional maximum ratings

		Conditions	Lower limit B	Upper limit A	Unit
Input current, each input, max. 4 inputs simultaneously	I_I	30 µs pulse, duty cycle = 1:100	−30	30	mA
Output current, each output	I_Q		−30	30	mA

Electrical characteristics, 12 V range

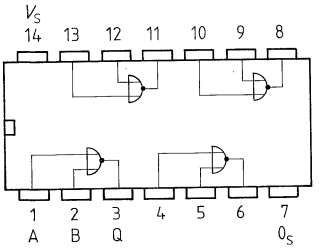
Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			11.4	15	17	V
H-input voltage	V_{IH}	$V_S = V_{SA}$ to V_{SB}	3	8		30	V
L-input voltage	V_{IL}	$V_S = V_{SA}$ to V_{SB}	3	0		4.5	V
H-output voltage	V_{QH}	$V_S = V_{SA}$ to V_{SB}, $-I_{QH} = 5$ mA	3	$V_S - 1.4$			V
L-output voltage	V_{QL}	$V_S = V_{SA}$ to V_{SB}, $I_{QL} = 1.8$ mA	3			1.7	V
	V_{QL}	$V_S = V_{SA}$ to V_{SB} $I_{QL} = 5.4$ mA	3			2.6	V
Input current	I_I	$V_I = 2$ V to 30 V	2	0.2	0.5	1	mA
	$-I_I$	$V_I = 0$ V	2			10	µA
Short circuit output current	$-I_{QH}$	$V_S = V_{SA}$, $V_Q = 0$ V	1	9	15	30	mA
	I_{QL}	$V_S = V_{SA}$, $V_Q = V_S$	1	5.5	10	25	mA
H-supply current	I_{SH}	$V_S = V_{SA}$, $V_I = 0$ V	6			12	mA
L-supply current	I_{SL}	$V_S = V_{SA}$, $V_I = V_{SA}$	7			20	mA
Z protection of inputs	V_{IZ}	$I_I \leqq 30$ mA, 30 µs pulse, duty cycle = 1:100	3	30			V
Input protection with series resistor	V_{IR}	$I_I \leqq 30$ mA, $R_S = 1$ kΩ		−30		60	V
Protective diodes at outputs and inputs in forward direction	V_{QF}	$I_Q \leqq 30$ mA	2+3			2	V

Dynamic characteristics

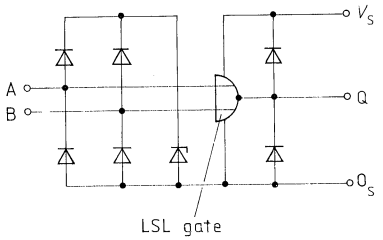
Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Propagation delay	t_{PLH}	$V_S = V_{SA}$ to V_{SB},				1	µs
	t_{PHL}	$C_L = 100\,pF$				1	µs
		$V_I = V_Q = 7\,V$,	26				
Transition time	t_{TLH}	input pulse: 10 V,				0.6	µs
	t_{THL}	t_{THL}, $t_{TLH} \leqq 1\,\mu s$				0.6	µs



Pin configuration
top view

Schematic (one gate)



Logic function $Q = \overline{A \wedge B}$

JK Master-Slave Flipflop

FZJ 101
FZJ 105
FZJ 111
FZJ 115

Type	Ordering code
FZJ 101	Q67000–J95
FZJ 105	Q67000–J124
FZJ 111	Q67000–J96
FZJ 115	Q67000–J125

FZJ 101/105: JK master-slave flipflop with two J and K-inputs and N-inputs on slave
FZJ 111/115: JK master-slave flipflop with N-inputs on master and slave

Electrical characteristics, 12 V range
Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	22	7.5			V
L-input voltage at any input except C	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4.5	V
L-input voltage at C	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA}, $V_{IL} = 4.5\,V$[1]), $-V_{QH} = 0.1\,mA$	22	10	11.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5\,V$[1]), $I_{QL} = 15\,mA$	22		1	1.7	V
DC noise margin							
H-signal	V_{nm}			2.5	5		V
L-signal	V_{nm}			2.8	5		V
H-input current at any input except C	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	23			1	µA
H-input current at C	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	23			3	µA
L-input current at any input except C	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$	24		0.8	1.5	mA
L-input current at C	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$	24		1.6	3	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_Q = 0\,V$	25	10	30	50	mA
Supply current	I_S	$V_S = V_{SA}$, $V_I = V_{IHA}$	23		8	14	mA

[1]) Measured at $\overline{R}$ or $\overline{S}$.

Delay times, $V_S = 12\,V$, $F_Q = 1$, $T_{amb} = 25°\,C$

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Maximum clock frequency	f	duty cycle 1:1		0.2	0.5		MHz
Clock pulse width	t_{pC}			0.6			µs
Reset pulse width	t_{pR}			1			µs
Set pulse width	t_{pS}	at 50 %		1			µs
Setup time	t_S			0			ns
Hold time	t_H			0			ns
Propagation delay from C to Q	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	31	160	290	520	ns
	t_{PHL}		31	270	450	770	ns
from $\overline{R}$ or $\overline{S}$ to Q	t_{PLH}		30	70	165	330	ns
	t_{PHL}		30	180	330	580	ns
Transition time at Q	t_{TLH}	$C_L = 10\,pF$	31	200	340	570	ns
	t_{THL}		31	70	120	210	ns

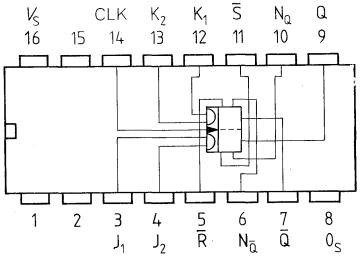
Electrical characteristics, 15 V range
Temperature range 1 and 5

Supply voltage	V_S			13.5	15	17	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	22	7.5			V
L-input voltage at any input expect C	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4.5	V
L-input voltage at C	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA}, $V_{IL} = 4.5\,V$[1]), $-V_{QH} = 0.1\,mA$	22	12	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5\,V$[1]), $I_{QL} = 18\,mA$	22		1.1	1.7	V
DC noise margin H-signal	V_{nm}			4.5	8		V
L-signal	V_{nm}			2.8	5		V
H-input current at any input except C	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	23			1	µA
H-input current at C	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	23			3	µA
L-input current at any input except C	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$	24		1	1.8	mA
L-input current at C	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$	24		2	3.6	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_Q = 0\,V$	25	25	37	60	mA
Supply current	I_S	$V_S = V_{SA}$, $V_I = V_{IHA}$	23		11	20	mA

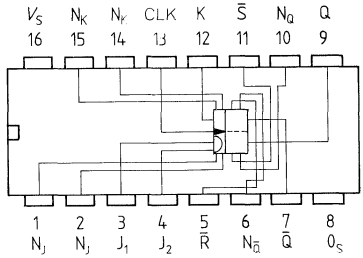
[1]) Measured at $\overline{R}$ or $\overline{S}$.

Delay times, $V_S = 15\,V$, $F_Q = 1$, $T_{amb} = 25°\,C$

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Propagation delay from CLK to Q	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	31		330		ns
	t_{PHL}		31		470		ns
from $\overline{R}$ or $\overline{S}$ to Q	t_{PLH}		30		195		ns
	t_{PHL}		30		340		ns
Transition time at Q	t_{TLH}	$C_L = 10\,pF$	31		410		ns
	t_{THL}		31		75		ns



FZJ 101, FZJ 105
Pin configuration
top view



FZJ 111, FZJ 115
Pin configuration
top view

Logic data

		Upper limit A
H-output load factor, each output	F_{QH}	100
L-output load factor, each output	F_{QL}	10
H-input load factor at CLK	F_{IH}	3
L-input load factor at CLK	F_{IL}	2
Input load factor of remaining inputs	F_I	1

$\overline{R}$ and $\overline{S}$ are approx. 1.5 normalized loads dynamically

Truth table

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

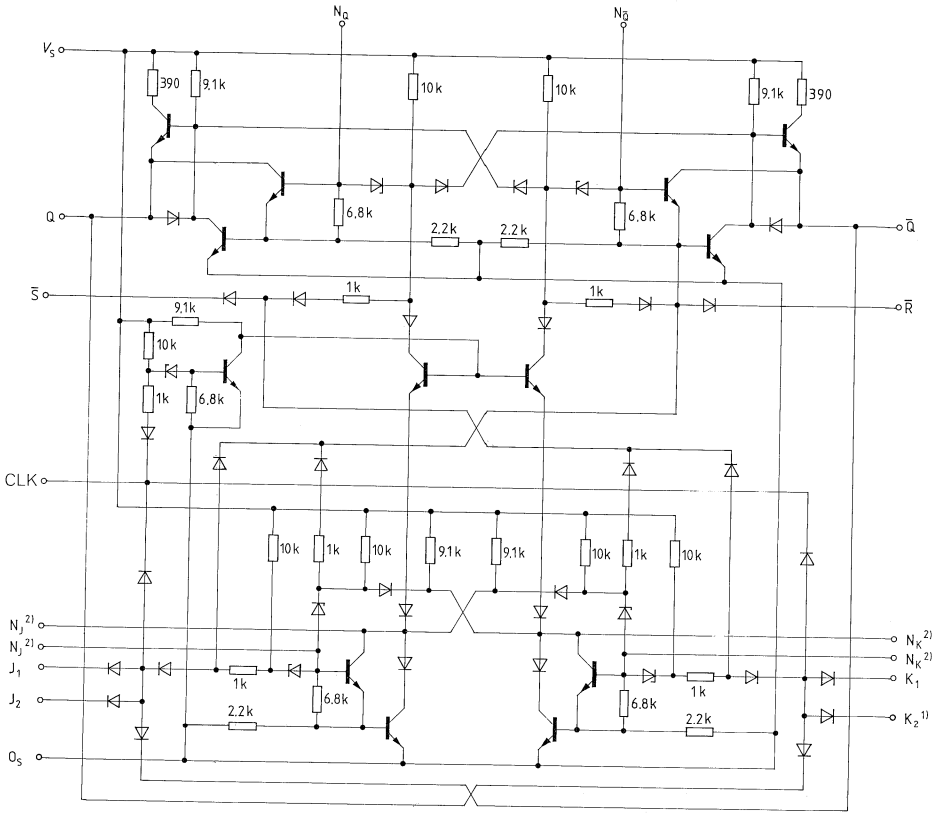
J = $J_1 \wedge J_2$
K = $K_1 \wedge K_2$, FZJ 101/FZJ 115 only
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

L-level at $\overline{R}$ sets Q to L
L-level at $\overline{S}$ sets Q to H
$\overline{R}$ and $\overline{S}$ operate independently of CLK

Clock pulse

1 Isolate slave from master
2 Enter signal from J and K into master
3 Disable inputs J and K
4 Transfer information from master to slave

Schematic



CLK = clock; J, K = inputs; Q, $\overline{Q}$ = outputs; $\overline{R}$ = reset; $\overline{S}$ = set

[1]) FZJ 101/105 only.
[2]) FZJ 111/115 only.

Type	Ordering code
FZJ 121	Q67000–J385
FZJ 125	Q67000–J386

Electrical characteristics, 12 V range

Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			11.4	12	13.5	V
H-input voltage at CLK, J and K	V_{IH}	$V_S = V_{SB}$	22	8			V
L-input voltage at CLK	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4	V
L-input voltage at J and K	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			5.5	V
H-input voltage at $\overline{R}$ and $\overline{S}$	V_{IH}	$V_S = V_{SB}$	22	7.5			V
L-input voltage at $\overline{R}$ and $\overline{S}$	V_{IL}	$V_S = V_{SB}$ and V_{SA} $-I_{QH} = 0.1$ mA	22			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA} $V_{IL} = 4.5$ V[1])	22	10	11.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5$ V[1]) $I_{QL} = 18$ mA	22		1	1.7	V
DC noise margin							
H-signal	V_{nm}			2	5		V
L-signal	V_{nm}			2.3	5		V
H-input current at CLK	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	23			3	µA
H-input current at J, K, $\overline{R}$ and $\overline{S}$	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	23			1	µA
L-input current at CLK	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V	24		1.6	3	mA
L-input current at J, K, $\overline{R}$ and $\overline{S}$	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V	24		0.8	1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_Q = 0$ V	25	9	15	25	mA
Supply current	I_S	$V_S = V_{SA}$, $V_I = V_{IHA}$	23		15	24	mA

[1]) Measured at $\overline{R}$ or $\overline{S}$.

Delay times, $V_S = 12\,V$, $F_Q = 1$, $T_{amb} = 25°C$

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Maximum clock frequency	f	duty cycle 1:1		0.2	0.5		MHz
Clock pulse width	t_{pC}	at 50 %		0.6			µs
Reset pulse width	t_{pR}			1			µs
Set pulse width	t_{pS}			1			µs
Setup time	t_S			0			ns
Hold time	t_H			0			ns
Propagation delay							
from CLK to Q	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	31	160	290	520	ns
	t_{PHL}		31	270	450	770	ns
from $\overline{R}$ or $\overline{S}$ to Q	t_{PLH}		30	70	165	330	ns
	t_{PHL}		30	180	330	580	ns
Transition time	t_{TLH}	$C_L = 10\,pF$	31	200	340	570	ns
at Q	t_{THL}		31	70	120	210	ns

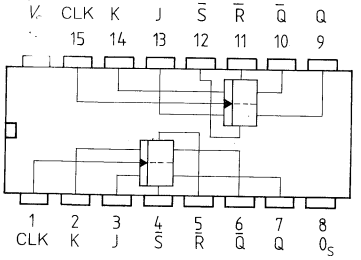
Electrical characteristics, 15 V range
Temperature range 1 and 5

Supply voltage	V_S			13.5	15	17	V
H-input voltage at CLK, J and K	V_{IH}	$V_S = V_{SB}$	22	8			V
L-input voltage at CLK	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4	V
L-input voltage at J and K	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			5.5	V
H-input voltage at $\overline{R}$ and $\overline{S}$	V_{IH}	$V_S = V_{SB}$	22	7.5			V
L-input voltage at $\overline{R}$ and $\overline{S}$	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA}, $V_{IL} = 4.5\,V$[1]), $-I_{QH} = 0.1\,mA$	22	12	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5\,V$[1]), $I_{QL} = 18\,mA$	22		1.1	1.7	V
DC noise margin							
H-signal	V_{nm}			4	8		V
L-signal	V_{nm}			2.3	5		V
H-input current at CLK	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	23			3	µA
H-input current at J, K, $\overline{R}$ and $\overline{S}$	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	23			1	µA
L-input current at CLK	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$	24		2	3.6	mA
L-input current at J, K, $\overline{R}$ and $\overline{S}$	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$	24		1	1.8	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_Q = 0\,V$	25	9	15	25	mA
Supply current	I_S	$V_S = V_{SA}$, $V_I = V_{IHA}$	23		20	32	mA

[1]) Measured at $\overline{R}$ or $\overline{S}$.

Delay times, $V_S = 15\,V$, $F_Q = 1$, $T_{amb} = 25°\,C$

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Propagation delay from CLK to Q	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	31		330		ns
	t_{PHL}		31		470		ns
from $\overline{R}$ or $\overline{S}$ to Q	t_{PLH}		30		195		ns
	t_{PHL}		30		340		ns
Transition time at Q	t_{TLH}	$C_L = 10\,pF$	31		410		ns
	t_{THL}		31		75		ns



Pin configuration
top view

Logic data, each flipflop

		Upper limit A
H-output load factor, each output	F_{QH}	100
L-output load factor, each output	F_{QL}	10
H-input load factor		
at CLK	F_{IH}	3
at $\overline{R}$ and $\overline{S}$	F_{IH}	1
L-input load factor at CLK, $\overline{R}$ and $\overline{S}$	F_{IL}	2
Remaining inputs	F_I	1

$\overline{R}$ and $\overline{S}$ are approx. 1.5 normalized loads dynamically

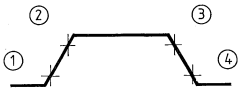
Truth table

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

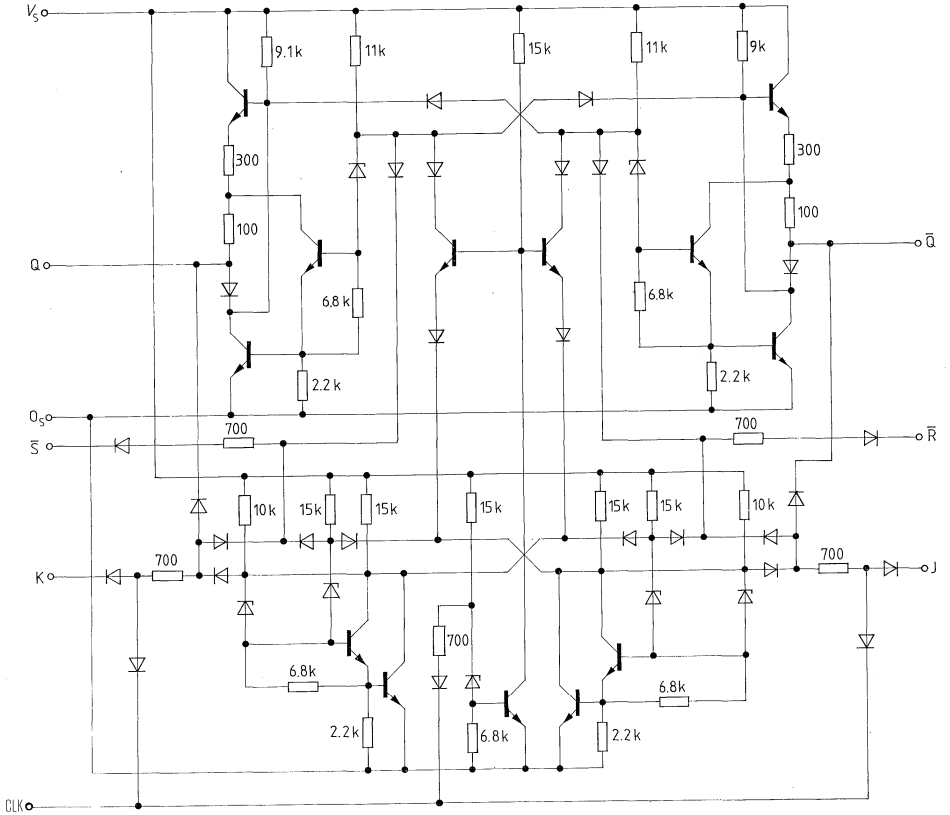
L-level at $\overline{R}$ sets Q to L
L-level at $\overline{S}$ sets Q to H
$\overline{R}$ and $\overline{S}$ operate independently of CLK

Clock pulse



1 Isolate slave from master
2 Enter signal from J and K into master
3 Disable inputs J and K
4 Transfer information from master to slave

Schematic



CLK = clock; J, K = inputs; Q, $\overline{Q}$ = outputs; $\overline{R}$ = reset; $\overline{S}$ = set

Type	Ordering code
FZJ 131	Q67000–J388
FZJ 135	Q67000–J389

The FZJ 131 and FZJ 135 contain four D-flipflops. Information present at the D-input is transferred to the Q-output while the clock input CLK is at H. The D-input is disabled at CLK = L.
Typical application: 4-bit temporary memory

Electrical characteristics, 12 V range

Temperature range 1 and 5

		Test conditions	Lower limit B	Typ	Upper limit A	Unit
Supply voltage	V_S		11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$, $-I_{QH} = 0.1$ mA, $V_{IH} = 7.5$ V	10	11.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $I_{QL} = 15$ mA, $V_{ID} = 4.5$ V, $V_{IC} = 7.5$ V		0.9	1.7	V
DC noise margin						
H-signal	V_{nm}		2.5	5		V
L-signal	V_{nm}		2.8	5		V
H-input current, each input	I_{IH}	$V_I = V_{IHA}$, $V_S = V_{SA}$			1	µA
L-input current at D	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V			3	mA
L-input current at CLK	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V			6	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_I = V_Q = 0$ V	9	15	25	mA
Supply current	I_S	$V_S = V_{SA}$, $V_I = 0$ V		22	32	mA
Power consumption	P	$V_S = V_{SA}$, $V_I = 0$ V		264	432	mW

Delay times, $V_S = 12$ V, $F_Q = 1$, $T_{amb} = 25°C$

Maximum clock frequency	f	duty cycle 1:1	0.5			MHz
Clock pulse width	t_{pC}	4.5 V above ground	0.5			µs
Setup time at D						
H-signal	t_S		300			ns
L-signal	t_S		500			ns
Hold time at D						
H-signal	t_H		150			ns
L-signal	t_H		50			ns
Propagation delay						
from D to Q	t_{PLH}	$C_L = 10$ pF at 4.5 V above ground	90	175	310	ns
	t_{PHL}		30	70	150	ns
from D to $\overline{Q}$	t_{PLH}		30	70	150	ns
	t_{PHL}		70	130	290	ns
from CLK to Q	t_{PLH}		90	160	310	ns
	t_{PHL}		70	120	210	ns
from CLK to $\overline{Q}$	t_{PLH}		90	150	310	ns
	t_{PHL}		70	120	210	ns
Transition time at Q	t_{TLH}	$C_L = 10$ pF	50	90	170	ns
	t_{THL}		15	35	60	ns

Electrical characteristics, 15 V range

Temperature range 1 and 5

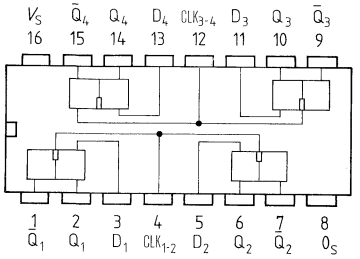
		Test conditions	Lower limit B	Typ	Upper limit A	Unit
Supply voltage	V_S		13.5	15	17	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$, $-I_{QH} = 0.1$ mA, $V_{IH} = 7.5$ V	12	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $I_{QL} = 18$ mA, $V_{ID} = 4.5$ V, $V_{IC} = 7.5$ V		1	1.7	V
DC noise margin						
H-signal	V_{nm}		4.5	8		V
L-signal	V_{nm}		2.8	5		V
H-input current, each input	I_{IH}	$V_I = V_{IHA}$, $V_S = V_{SA}$			1	µA
L-input current at D	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V			3.6	mA
L-input current at CLK	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V			7.2	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_I = V_Q = 0$ V	9	15	25	mA
Supply current	I_S	$V_S = V_{SA}$, $V_I = 0$ V		28	42	mA
Power consumption	P	$V_S = V_{SA}$, $V_I = 0$ V		420	720	mW

Delay times, $V_S = 15$ V, $F_Q = 1$, $T_{amb} = 25°$ C

Propagation delay						
from D to Q	t_{PLH}	$C_L = 10$ pF at 4.5 V above ground		210		ns
	t_{PHL}			65		ns
from D to $\overline{Q}$	t_{PLH}			65		ns
	t_{PHL}			125		ns
from CLK to Q	t_{PLH}			195		ns
	t_{PHL}			115		ns
from CLK to $\overline{Q}$	t_{PLH}			205		ns
	t_{PHL}			100		ns
Transition time at Q	t_{TLH}	$C_L = 10$ pF		115		ns
	t_{THL}			25		ns

Logic data, each flipflop

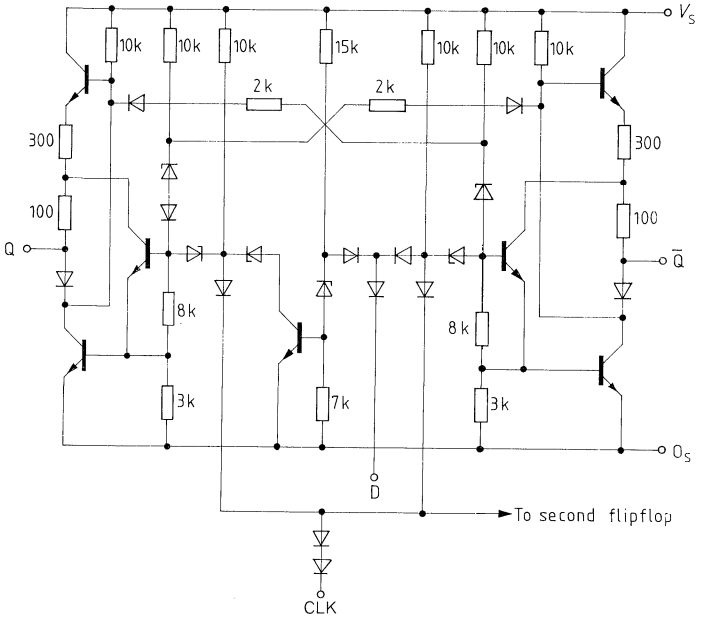
H-output load factor each output	F_{QH}		100
L-output load factor each output	F_{QL}		10
Input load factor at D	F_I		2
Input load factor at CLK	F_I	for 2 flipflops	4



Pin configuration
top view

CLK = Clock input
D = Data input
Q, $\bar{Q}$ = Outputs

Schematic (one flipflop)



Truth table (each flipflop)

Input CLK	D_n	Output Q_{n+1}
L	L	Q_n
L	H	Q_n
H	L	L
H	H	H

n: bit time before clock pulse
n + 1: bit time after clock pulse

Type	Ordering code
FZJ 141 A	Q67000–J642
FZJ 145 A	Q67000–J647
FZJ 151 A	Q67000–J684
FZJ 155 A	Q67000–J685

FZJ 141 A/145 A: Synchronous decimal counter with N-input
FZJ 151 A/155 A: Synchronous 4-bit binary counter with N-input

The FZJ 141 A/145 A and FZJ 151 A/155 A are synchronous counters with set inputs for each bit, a common reset input, clock disabling, and carry gating. The information is stored in JK-flipflops and is available at the output Q with the trailing edge of the clock pulse.

The principle of operation of the counter is shown in pulse diagrams.

Electrical characteristics, 12 V range
Temperature range 1 and 5

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			11.4	12	13.5	V
H-input voltage at E and CLK	V_{IH}			8			V
at $\overline{A}$,$\overline{B}$,$\overline{C}$,$\overline{D}$, and $\overline{R}$	V_{IH}	$V_S = V_{SB}$		7.5			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ and V_{SB}				4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$, $-I_{QH} = 0.1$ mA		10	11.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $I_{QL} = 15$ mA			0.9	1.7	V
DC noise margin H-signal	V_{nm}			2.5	5		V
L-signal	V_{nm}			2.8	5		V
H-input current each input	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$				1	µA
L-input current each input	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V			0.8	1.5	mA
Short-circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_Q = 0$ V		9	15	25	mA
H-supply current	I_{SH}	$V_S = V_{SA}$, $V_I = V_{SA}$			12	17	mA
L-supply current	I_{SL}	$V_S = V_{SA}$ Input $\overline{R}$: $V_I = 0$ V Remaining inputs: $V_I = V_{SA}$			20	29	mA

Delay times, $V_S = 12\,V$, $F_Q = 1$, $T_{amb} = 25°\,C$

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Capacitance	C_N			0		1	nF
Clock pulse width	t_{pC}	4.5 V above ground		0.5			µs
Maximum clock frequency	f	duty cycle 1:1		0.5	1.5		MHz
Reset pulse width	t_{pR}			0.5			µs
Recovery time after reset by $\overline{R}$, referred to HL clock pulse transition	t_{rR}	4.5 V above ground	53			2	µs
Reset pulse width during set operation	t_{pR}		54	1			µs
Setup time at $\overline{A}, \overline{B}, \overline{C}, \overline{D}$	t_S		54	1			µs
Hold time at $\overline{A}, \overline{B}, \overline{C}, \overline{D}$	t_H		54	1			µs
Propagation delay from CLK to Q	t_{PLH}		50	90	200	450	ns
	t_{PHL}		50	90	200	450	ns
from CLK to $\overline{Q}$	t_{PLH}		50	200	400	700	ns
	t_{PHL}		50	150	300	500	ns
from E_C to C_Q	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	52	90	200	450	ns
	t_{PHL}		52	25	60	200	ns
from $\overline{R}$ to Q	t_{PHL}		53	70	150	310	ns
from $\overline{A}$ to Q_A,	t_{PLH}		51	30	120	210	ns
$\overline{B}$ to Q_B, $\overline{C}$ to Q_C, $\overline{D}$ to Q_D	t_{PHL}		51	30	120	210	ns
Transition time at CLK	t_T			1			V/µs
at Q	t_{TLH}			90	250	450	ns
	t_{THL}			5	20	60	ns
at C_Q	t_{TLH}	$C_L = 10\,pF$	50	70	140	310	ns
	t_{THL}			30	60	210	ns

Electrical characteristics, 15 V range

Temperature range 1 and 5

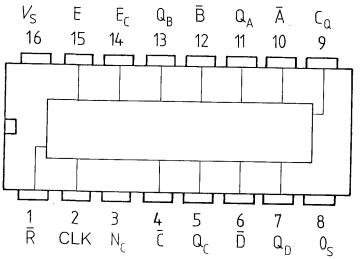
		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S			13.5	15	17	V
H-input voltage at E and CLK	V_{IH}			8			V
at $\overline{A}$,$\overline{B}$,$\overline{C}$,$\overline{D}$, and $\overline{R}$	V_{IH}	$V_S = V_{SB}$		7.5			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ and V_{SB}				4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$, $-I_{QH}$ = 0.1 mA		12	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, I_{QL} = 18 mA			1	1.7	V
DC noise margin							
H-signal	V_{nm}			4.5	8		V
L-signal	V_{nm}			2.8	5		V
H-input current each input	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$				1	µA
L-input current each input	$-I_{IL}$	$V_S = V_{SA}$, V_I = 1.7 V			1	1.8	mA
Short-circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, V_Q = 0 V		9	15	25	mA
H-supply current	I_{SH}	$V_S = V_{SA}$, $V_I = V_{SA}$			15	23	mA
L-supply current	I_{SL}	$V_S = V_{SA}$, Input $\overline{R}$: V_I = 0 V, Remaining inputs: $V_I = V_{SA}$			23	36.5	mA

Delay times, V_S = 15 V, F_Q = 1, T_{amb} = 25° C

		Test conditions	Test circuit	Lower limit B	Typ.	Upper limit A	Unit
Propagation delay from CLK to Q	t_{PLH}	C_L = 10 pF at 4.5 V above ground	50				ns
	t_{PHL}						ns
from CLK to C_Q	t_{PLH}						ns
	t_{PHL}						ns
from E_C to C_Q	t_{PLH}		52				ns
	t_{PHL}		52				ns
from $\overline{R}$ to Q	t_{PHL}		53				ns
from $\overline{A}$ to Q_A,	t_{PLH}		51				ns
$\overline{B}$ to Q_B, $\overline{C}$ to Q_C, $\overline{D}$ to Q_D	t_{PHL}		51				ns
Transition times at CLK	t_T	C_L = 10 pF	50	1			V/µs
at Q	t_{TLH}						ns
	t_{THL}						ns
at C_Q	t_{TLH}						ns
	t_{THL}						ns

Logic data

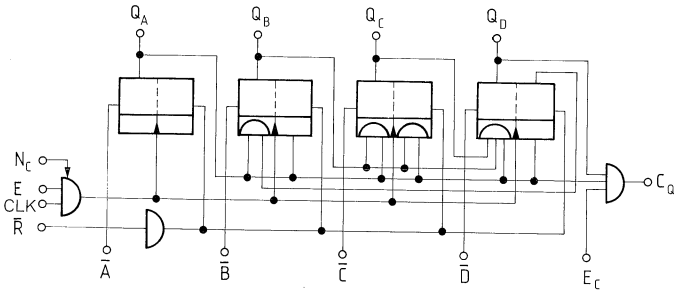
H-output load factor each output	F_{QH}		100
L-output load factor each output	F_{QL}		10
Input load factor, each input	F_I		1



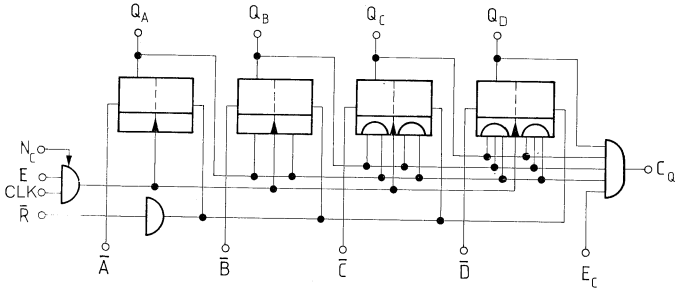
Pin configuration
top view

$\overline{A}, \overline{B}, \overline{C}, \overline{D}$ = Set inputs
CLK = Clock input
C_Q = Carry output
$\overline{E}$ = Enable input
$\overline{R}$ = Reset input
$Q, \overline{Q}$ = Outputs

Block diagram of FZJ 141 A/145 A



Block diagram of FZJ 151 A/155 A



Truth table: Decimal counter
FZJ 141 A/145 A

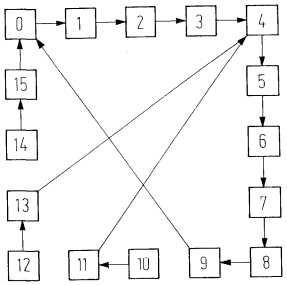
Count condition:
$\overline{A} = \overline{B} = \overline{C} = \overline{D} = \overline{E} = E_C = \overline{R} = H$

Sequence	Outputs				
	C_Q	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	H	H	L	L	H

Truth table: Binary counter
FZJ 151 A/155 A

Count condition:
$\overline{A} = \overline{B} = \overline{C} = \overline{D} = \overline{E} = E_C = \overline{R} = H$

Sequence	Outputs				
	C_Q	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	L	H	L	L	H
10	L	H	L	H	L
11	L	H	L	H	H
12	L	H	H	L	L
13	L	H	H	L	H
14	L	H	H	H	L
15	H	H	H	H	H



The adjacent flow graph shows the operation of the FZJ 141 A/145 A when set to values in the range 10 through 15

Enable conditions

Enable E	Operating mode
L	inhibit
H	count

Enable E_C	Carry output C_Q
L	L
H	L or H

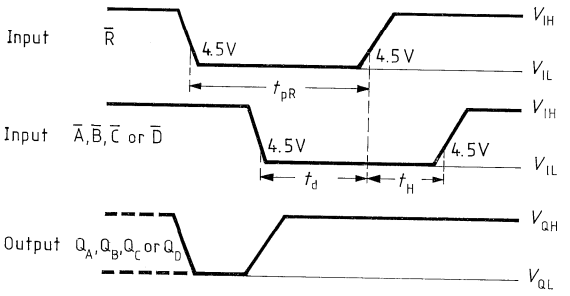
Set and reset inputs operate independently of the clock input CLK and the enable input E. If these inputs are not used, they must be connected to V_S. To store the information at $\overline{A}$through $\overline{D}$ properly $\overline{R}$ must return to H-level before the inputs $\overline{A}$ through $\overline{D}$.

Set and reset conditions

Inputs					Outputs			
$\overline{R}$	$\overline{A}$	$\overline{B}$	$\overline{C}$	$\overline{D}$	Q_A	Q_B	Q_C	Q_D
L	H	H	H	H	L	L	L	L
L	L	X	X	X	H	X	X	X
L	X	L	X	X	X	H	X	X
L	X	X	L	X	X	X	H	X
L	X	X	X	L	X	X	X	H

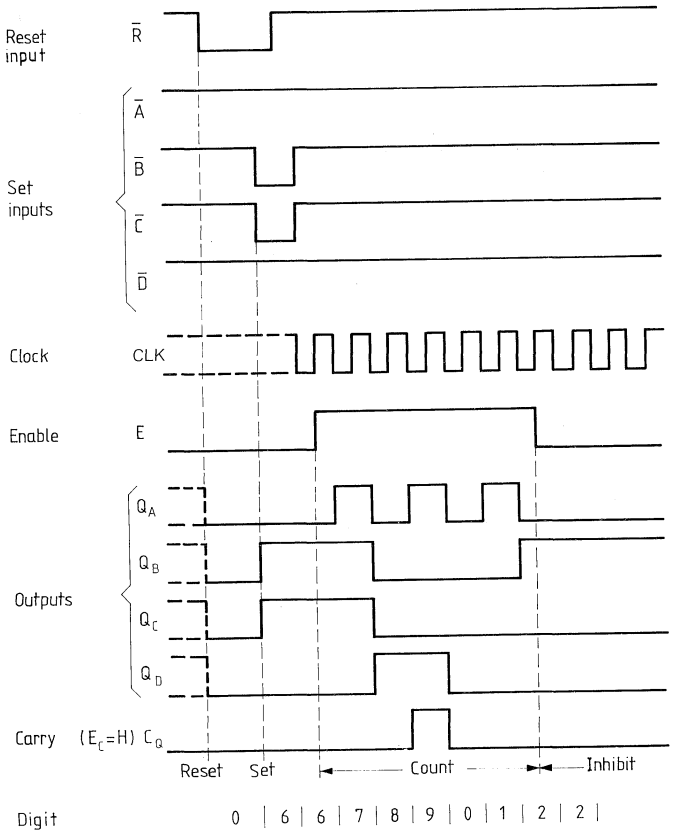
X = L- or H-signal

Pulse diagram for set operation



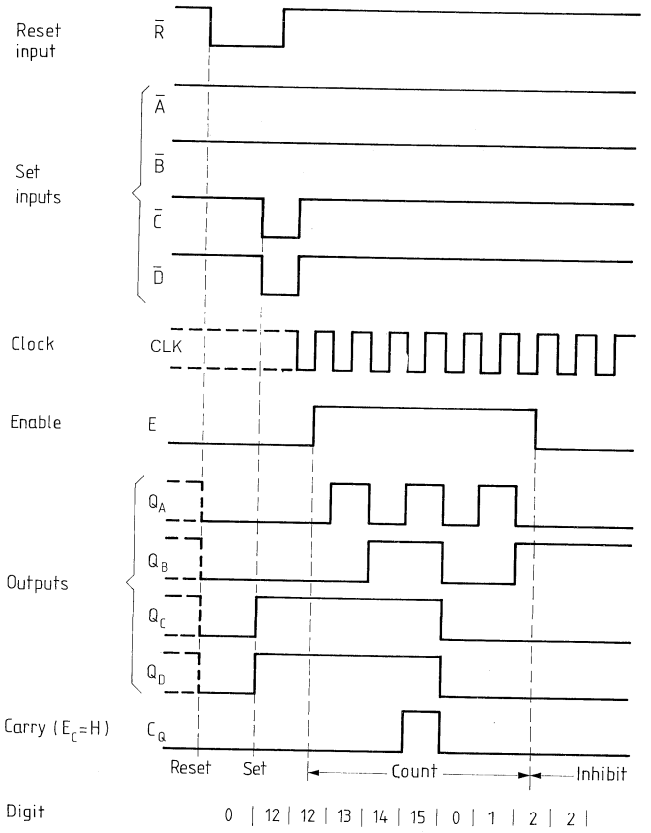
Pulse diagram for the decimal counter FZJ 141 A/145 A, with the following functions:

1. Reset to Q = L
2. Set to binary 6
3. Count from binary 6 to 2 with carry pulse
4. Inhibit



Pulse diagram for the binary counter FZJ 151 A/155 A with the following functions:

1. Reset to Q = L
2. Set to binary 12
3. Count from binary 12 to 2 with carry pulse
4. Inhibit



Synchronous 4-Bit Shift Register with Set and Reset Inputs and N-Input

Type	Ordering code
FZJ 161	Q67000–J507
FZJ 165	Q67000–J562

The FZJ 161 and FZJ 165 are synchronous 4-bit shift registers with series or parallel inputs and series or parallel outputs for right shift operation. The principle of operation of the register is shown in the pulse diagram.
The shift registers are suitable for use as series-parallel converter, parallel-series converter, register, and buffer.

Electrical characteristics, 12 V range

Temperature range 1 and 5

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S		11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$, $-I_{QH} = 0.1$ mA, $V_{IL} = 4.7$ V	10	11.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $I_{QL} = 15$ mA		0.9	1.7	V
DC noise margin						
H-signal	V_{nm}		2.5	5		V
L-signal	V_{nm}		2.8	5		V
H-input current, each input	I_{IH}	$V_I = V_{IHA}$, $V_S = V_{SA}$			1	µA
L-input current, each input	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V			1.5	mA
L-input current at S	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V			6	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_I = V_Q = 0$ V	9	15	25	mA
Supply current	I_S	$V_S = V_{SA}$, $V_I = 0$ V		21	33	mA

Delay times, $V_S = 12\,V$, $F_Q = 1$, $T_{amb} = 25°C$

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Capacitance	C_N		0		1	nF
Maximum clock frequency	f	duty cycle 1:1	0.5	1.5		MHz
Clock pulse width	t_{pC}		0.5			µs
Reset pulse width	t_{pR}		0.5			µs
Reset pulse width during set operation	t_{pR}		1			µs
Setup time at A, B, C, D, S	t_S	4.5 V above ground	1			µs
Setup time at SI	t_S		0			µs
Hold time at A, B, C, D, S	t_H		1			µs
Hold time at SI	t_H		0.5			µs
Propagation delay from CLK to Q	t_{PLH}		90	140	450	ns
	t_{PHL}		90	140	450	ns
from $\overline{R}$ to Q	t_{PHL}	$C_L = 10\,pF$ at 4.5 V above ground	0.6	0.85	1.3	µs
from S to Q, A to Q_A, B to Q_B,	t_{PLH}		100	240	500	ns
C to Q_C, D to Q_D	t_{PHL}		90	140	450	ns
Transition times at CLK	t_T		1			V/µs
at Q	t_{TLH}	$C_L = 10\,pF$	70	150	290	ns
	t_{THL}		5	20	60	ns

Electrical characteristics, 15 V range

Temperature range 1 and 5

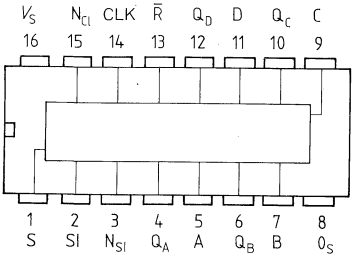
		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S		13.5	15	17	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$, $-I_{QH} = 0.1$ mA, $V_{IL} = 4.5$ V	12	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $I_{QL} = 18$ mA		1	1.7	V
DC noise margin						
H-signal	V_{nm}		4.5	8		V
L-signal	V_{nm}		2.8	5		V
H-input current, each input	I_{IH}	$V_I = V_{IHA}$, $V_S = V_{SA}$			1	µA
L-input current, each input	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V			1.8	mA
L-input current at S	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V			7.2	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_I = V_Q = 0$ V	9	15	25	mA
Supply current	I_S	$V_S = V_{SA}$, $V_I = 0$ V		26	42	mA

Delay times, $V_S = 15$ V, $F_Q = 1$, $T_{amb} = 25°$ C

Propagation delay from CLK to Q	t_{PLH}	$C_L = 10$ pF at 4.5 V above ground				ns
	t_{PHL}					ns
from $\overline{R}$ to Q	t_{PHL}					µs
from S to Q, A to Q_A, B to Q_B,	t_{PLH}					ns
C to Q_C, D to Q_D	t_{PHL}					ns
Transition times						
at CLK	t_T	$C_L = 10$ pF	1			V/µs
at Q	t_{TLH}					ns
	t_{THL}					ns

Logic data

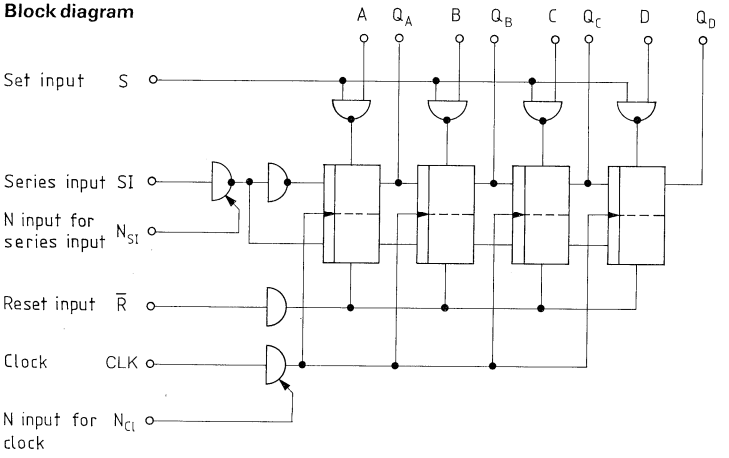
H-output load factor each output	F_{QH}		100
L-output load factor each output	F_{QL}		10
Input load factor at S,	F_I		4
remaining inputs	F_I		1



Pin configuration
top view

A, B, C, D = Inputs
CLK = Clock input
Q = Outputs
$\overline{R}$ = Reset input
S = Set input
SI = Series input

Block diagram



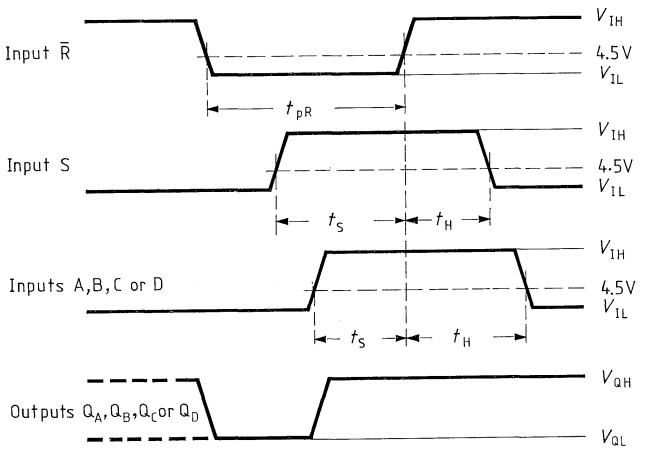
Set and reset conditions

Set and reset inputs operate independently of the clock input CLK. To store the parallel information properly, $\overline{R}$ must return to H-level before S is switched to L-level.

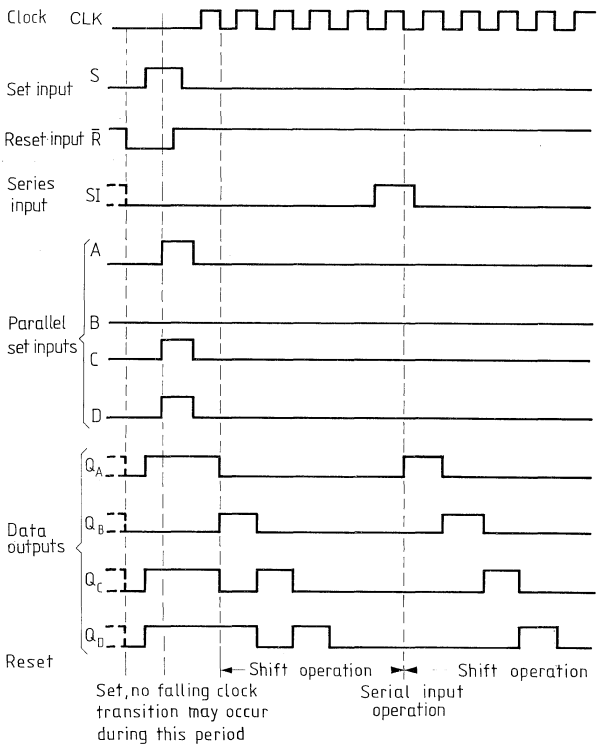
Inputs						Outputs				Function
S	$\overline{R}$	A	B	C	D	Q_A	Q_B	Q_C	Q_D	
L	L	X	X	X	X	L	L	L	L	reset
H	L	H	L	H	H	H	L	H	H	set
L	H	X	X	X	X					shift
H	H	H	H	L	L	L	L	X	X	undefined

X = L or H signal

Pulse diagram for set operation



Pulse diagram



Type	Ordering code
FZK 101	Q67000–K6
FZK 105	Q67000–K7

The timing circuits FZK 101 and FZK 105 have the following electrical functions and characteristics:

1. Monostable flipflop: L, J, and M connected.
2. Pulse delay: L and K connected.
3. Pulse reduction: J and M connected.
4. Delay switch: L–K and M–O_S connected.
5. The pulse delay is retriggerable if the pulse interval fulfills the condition $t_p > t_r$.
6. An electrolytic capacitor can be used as the timing component C_t.
7. After connection of the supply voltage V_S, Q is at L level if $\overline{R}$ was at L level during switching on.
8. No voltages or currents may be connected to the function inputs J, K, L, M. The necessary connections between these inputs for selection of the function must be kept as short as possible (max. 5 mm).
9. If inputs C and D are used as inputs, then input A or B must be supplied with L level.
10. An additional capacitor is connected between N input and ground.

Electrical characteristics, 12 V range
Temperature range 1 and 5

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S		11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA}, $V_{IL} = 4.5\,V$, $-I_{QH} = 0.1\,mA$	10	11.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5\,V$ $I_{QL} = 15\,mA$		1	1.7	V
DC noise margin						
H-signal	V_{nm}		2.5	5		V
L-signal	V_{nm}		2.8	5		V
H-input current, each input	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$			1	µA
L-input current, each input	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$		0.8	1.5	mA
Short circuit output current	$-I_Q$	$V_S = V_{SA}$	9	15	25	mA
L-supply current	I_{SL}			13	19	mA
H-supply current	I_{SH}			12	19	mA

Electrical characteristics, 15 V range

Temperature range 1 and 5

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S		13.5	15	17	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA}, $V_{IL} = 4.5\,V$, $-I_{QH} = 0.1\,mA$	12	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5\,V$, $I_{QL} = 18\,mA$		1.1	1.7	V
DC noise margin						
H-signal	V_{nm}		4.5	8		V
L-signal	V_{nm}		2.8	5		V
H-input current, each input	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$			1	µA
L-input current, each input	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7\,V$		1	1.8	mA
Short circuit output current	$-I_Q$	$V_S = V_{SA}$	9	15	25	mA
H-supply current	I_{SH}			14	22	mA
L-supply current	I_{SL}			15	23	mA

Delay times, $V_S = 12\,V$, $F_Q = 1$, $T_{amb} = 25°C$

Input pulse width	t_{pI}		0.5			µs
Reset pulse width	t_{pR}		0.5			µs
Setup time at A, B	t_S		0			µs
Setup time at C, D	t_S		0.5			ms
Recovery time	t_r			$(C_0 + C_t) \times 10^3$		s/F
Min. output pulse width	t_p		400			ns
Output pulse width	t_p	$V_S = 11.4\,V$, $R_t = 0.5\,M\Omega$, $C_t = 2\,nF$	650	700	780	µs
Propagation delay						
from A, B, C, D to Q	t_{PLH}	$C_L = 10\,pF$ at 4.5 V above ground	220	270	740	ns
	t_{PHL}		110	180	450	ns
from $\overline{R}$ to Q	t_{PHL}		150	300	550	ns
Transition times						
at A, B	t_{TLH}		0.1			V/µs
at C, D	t_{THL}		1			V/µs
at Q	t_{TLH}	$C_L = 10\,pF$	50	100	200	ns
	t_{THL}		30	80	150	ns

Timing components

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Resistance	R_t		5		500	kΩ
Recommended resistance range for high accuracy	R_t		40		200	kΩ
Capacitance	C_t	Nom. voltage > 10 V		No limitation		
Capacitance	C_N		0		500	pF
Internal capacitance between H and O_S	C_O			10		pF

Logic data

H-output load factor	F_{QH}				100	
L-output load factor	F_{QL}				10	
Input load factor each input	F_I				1	

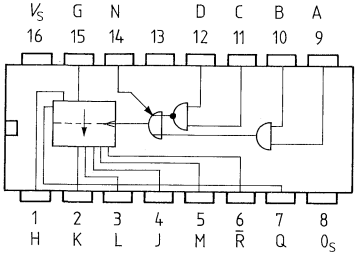
Logic function: $Q = (A \wedge B) \vee (\overline{C \wedge D})$, see pulse diagram

Truth table

Inputs A	B	C	D	Output Q
L	X	H	H	L
X	L	H	H	L
H	H	X	X	L
X	X	L	X	L
X	X	X	L	L
⌐	H	H	H	⌐¬
H	⌐	H	H	⌐¬
L	X	¬	H	⌐¬
L	X	H	¬	⌐¬
X	L	¬	H	⌐¬
X	L	H	¬	⌐¬

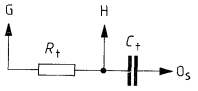
Notes

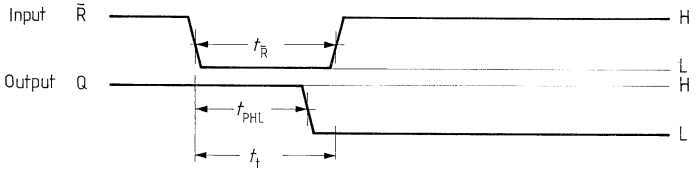
X = L or H signal
⌐¬ = H pulse with adjustable width
⌐ = L-H transition
¬ = H-L transition
Output Q refers to operation as monostable multivibrator. It applies accordingly to the remaining operating modes.



Pin configuration
top view

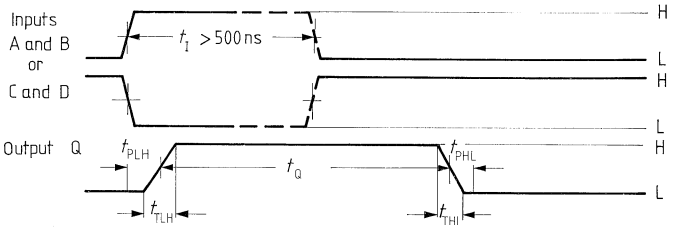
A, B, C, D = Inputs
J, K, L, M = Function inputs
Q = Output
$\overline{R}$ = Reset





Pulse diagrams for:

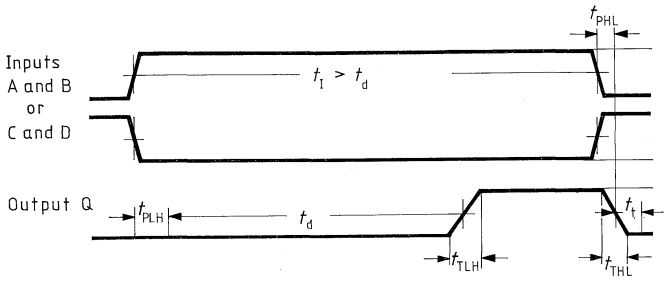
Reset with $\overline{R}$ (applies to every operating mode)



Monostable multivibrator
(L, J, and M connected)

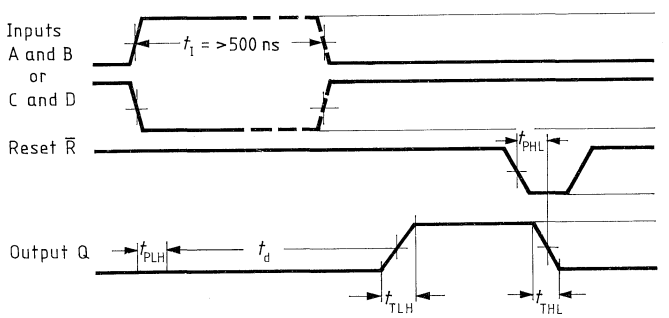
$t_Q = 0.7 \cdot R_t \cdot (C_0 + C_t)$

Pulse diagrams for:



Pulse delay
(L and K connected)

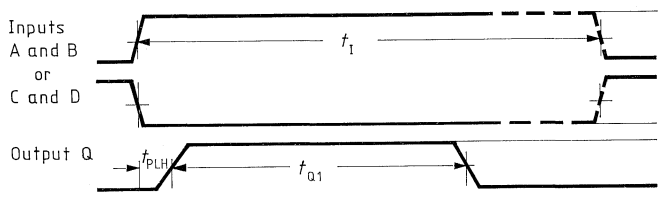
$t_d = 0.7 \cdot R_t \cdot (C_0 + C_t)$



Delay switch
(L–K and M–O_S connected)

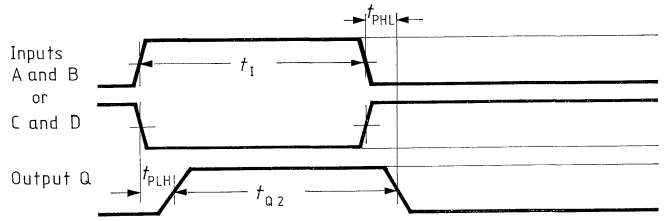
Reset to Q = L by means of $\overline{R}$ = L only

$t_d = 0.7 \cdot R_t \cdot (C_0 + C_t)$



Pulse reduction
(J and M connected)
a) $t_I > 0.7 \cdot R_t \cdot (C_0 + C_t)$

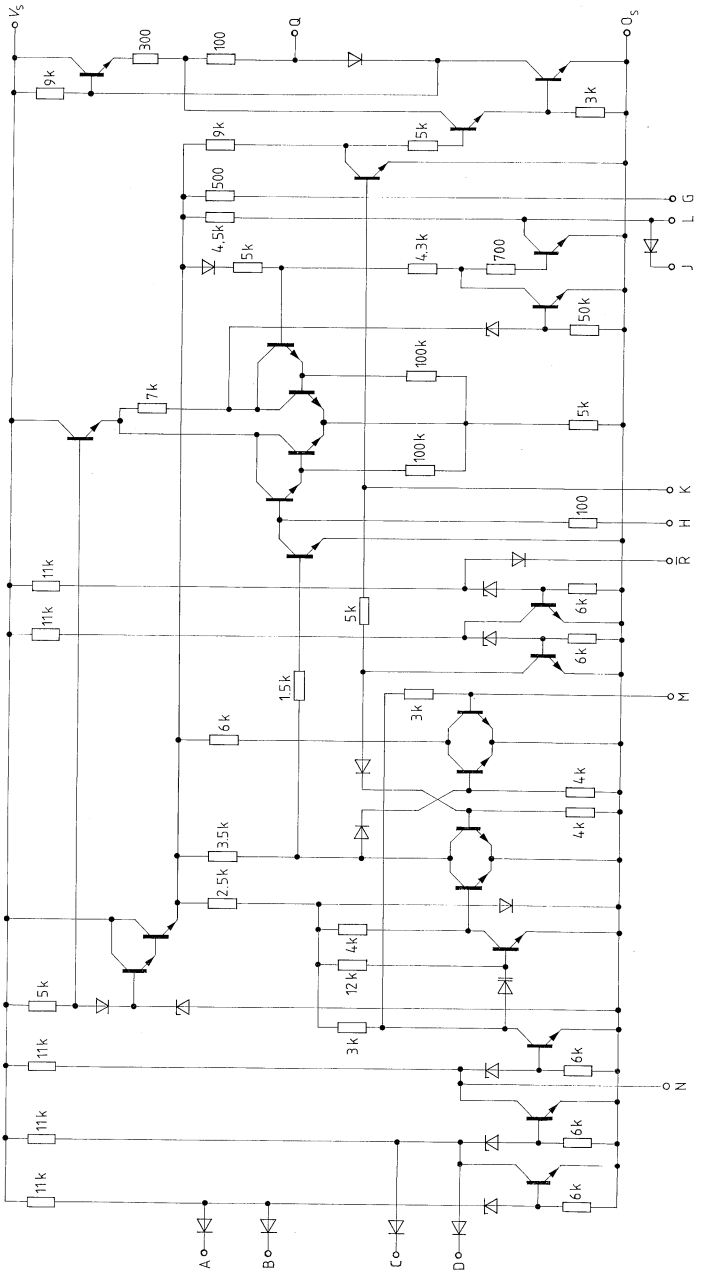
$t_{Q1} = 0.7 \cdot R_t \cdot (C_0 + C_t)$



b) $t_I \leqq 0.7 \cdot R_t \cdot (C_0 + C_t)$

$t_{Q2} = t_I$

Schematic


V_S
Q
Q_S
300
100
9k
3k
9k
5k
500
4.5k
5k
4.3k
700
50k
100k
7k
5k
100k
100
11k
11k
5k
6k
6k
1.5k
3k
6k
4k
4k
3.5k
2.5k
4k
12k
5k
3k
6k
11k
11k
6k
11k
6k
A
B
C
D
G
L
J
K
H
R
M
N

Type	Ordering code
FZL 101	Q67000-L68
FZL 105	Q67000-L69

The FZL 101 and FZL 105 decode binary coded decimal numbers. Direct control of indicator tubes is possible by means of output transistors with high breakdown voltages. The FZJ 141A is the corresponding decimal counter. The following connections have to be made from the Q-outputs of the FZJ 141A to the inputs of the FZL 101A: Q_A to A, Q_B to B, Q_C to C, and Q_D to D. Binary input information of the decimal numbers 10 to 15 is suppressed.

In addition the following **maximum ratings** apply:

		Lower limit B	Upper limit A	Unit
Output voltage (output transistor blocked)	V_Q	0	65	V
Output current (output transistor blocked), each output	I_Q	0	2	mA
Output current (output transistor conducting), each output	I_Q	0	20	mA

Electrical characteristics, 12 V range
Temperature range 1 and 5

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S		11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	8			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}			5	V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $I_{QL} = 9$ mA			2.5	V
DC noise margin						
H-signal	V_{nm}		2	4.5		V
L-signal	V_{nm}		3.3	5.5		V
Output current, each output	I_Q	$V_S = V_{SA}$, $V_Q = 65$ V			100	µA
	I_Q	$V_S = V_{SA}$, $V_Q = 60$ V			5	µA
H-input current, each input	I_{IH}	$V_S = V_I = V_{SA}$			1	µA
L-input current, each input	$-I_{IL}$	$V_S = V_{SA}$, $V_I = 0$ V		0.8	1.5	mA
Supply current	I_S	$V_S = V_{SA}$ Input A, C, D: $V_I = 0$ V		17	25	mA
Power consumption	P	Input B: $V_I = V_{SA}$		205	340	mW

Delay times, $V_S = 12\,V$, $T_{amb} = 25°\,C$

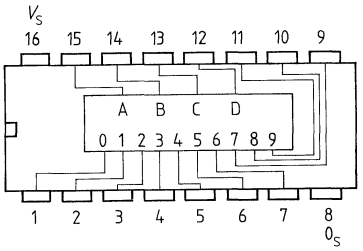
		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Propagation delay						
from B to dec 2	t_{PLH}	$V_{SC} = 12\,V$	30	70	210	ns
	t_{PHL}	$R_C = 1\,k\Omega$	60	150	280	ns
from B to dec 0	t_{PLH}	$C_L = 10\,pF$	60	150	280	ns
	t_{PHL}		30	70	210	ns

Electrical characteristics, 15 V range
Temperature range 1 and 5

Supply voltage	V_S		13.5	15	17	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	8			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}			5	V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $I_{QL} = 9\,mA$			2.5	V
DC noise margin						
H-signal	V_{nm}		4	7.5		V
L-signal	V_{nm}		3.3	5.5		V
H-output current, each output	I_Q	$V_S = V_{SA}$, $V_Q = 65\,V$			100	µA
	I_Q	$V_S = V_{SA}$, $V_Q = 60\,V$			5	µA
H-input current, each input	I_{IH}	$V_S = V_I = V_{SA}$			1	µA
L-input current, each input	$-I_{IL}$	$V_S = V_{SA}$, $V_I = 0\,V$		1	1.8	mA
Supply current	I_S	$V_S = V_{SA}$		18	27	mA
		Input A, C, D: $V_I = 0\,V$				
Power consumption	P	Input B: $V_I = V_{SA}$		270	460	mW

Delay times, $V_S = 15\,V$, $T_{amb} = 25°\,C$

Propagation delay						
from B to dec 2	t_{PLH}	$V_{SC} = 12\,V$		90		ns
	t_{PHL}	$R_C = 1\,k\Omega$		160		ns
from B to dec 0	t_{PLH}	$C_L = 10\,pF$		160		ns
	t_{PHL}			90		ns

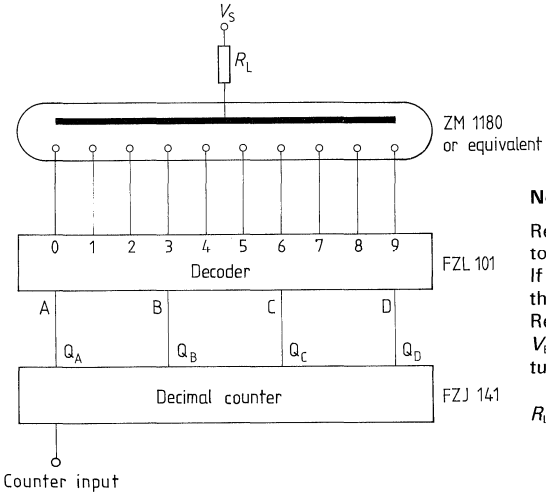


Pin configuration
top view

Truth table

BCD inputs				Decimal outputs									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

Application with indicator tube

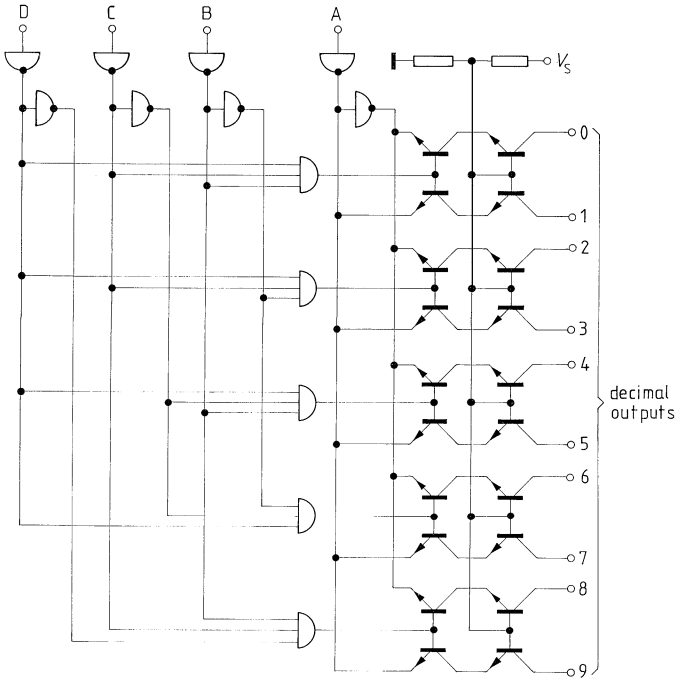


Notes:

Recommended supply voltage for the indicator tube $V_S = 200\,V$
If the input combinations 10 to 15 do not exist, then V_S is determined by the type of tube used.
Resistance R_L depends on the lighting voltage V_B and the lighting current I_B of the indicator tube according to the following equation:

$$R_L = \frac{V_S - V_B}{I_B}\,\Omega$$

Block diagram



BCD 7-Segment Decoder Driver incl. Open Collector Output with 16.5 V/20 mA

Type	Ordering code
FZL 111	Q67000-L156

The FZL 111 accepts binary coded 4-bit words, decodes them, depending on the conditional inputs (A, B, C, D, BI, RBI, LT) and drives the segments of a 7-segment display via the outputs a, b, c, d, e, f, g.
An L signal at the ripple blanking input RBI suppresses the decimal zero signal. In case of multidigit figures, the ripple blanking output RBQ (connected internally to input BI) provides automatic zero suppression over several decades. A signal at the blanking input BI blocks all outputs. A signal connected to the lamp test input LT permits checking of the display tubes (by lighting all segments). In addition to the maximum ratings specified in the introduction, the following apply:

Maximum ratings

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Output voltage for outputs a to g	V_Q	T_Q blocked	0		16.5	V
Output current	I_Q	T_Q blocked	0		25	µA
Output current for outputs a to g	I_{QL}	T_Q conducting	0		20	mA
outputs a to g	I_{QL}	T_Q conducting	0		40	mA
		Pulsed operation 1:1				

Electrical characteristics, 12 V range

Temperature range 1

Supply voltage	V_S		11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}			4.5	V
L-output voltage for outputs a to g	V_{QL}	$I_{QL} = 20$ mA, $V_S = V_{SB}$		0.4	0.7	V
	V_{QL}	$I_{QL} = 40$ mA*), $V_S = V_{SB}$		0.7	1	V
output BI/RBQ	V_{QL}	$I_{QL} = 7.5$ mA, $V_S = V_{SB}$			1.7	V
Output voltage for outputs a to g	V_Q	$V_S = V_{SB}$, $I_Q = 25$ µA			16.5	V
H-output voltage at BI/RBQ	V_{QH}	$V_S = V_{SA}$, $-I_{QH} = 0.1$ mA	10	11.3		V
DC noise margin						
H-signal	V_{nm}		2.5	5		V
L-signal	V_{nm}		2.8	5		V
H-input current						
at A, B, C, D, RBI	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$			10	µA
at BI/RBQ	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$			20	µA
at LT	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$			30	µA

*) Duty cycle 1:1

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
L-input current						
at A, B, C, D, RBI	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V		1	2.1	mA
at BI/RBQ	$-I_{IL}$			2	4.2	mA
at LT	$-I_{IL}$			3	6.3	mA
Supply current	I_S	$V_S = V_{SA}$, outputs open			40	mA

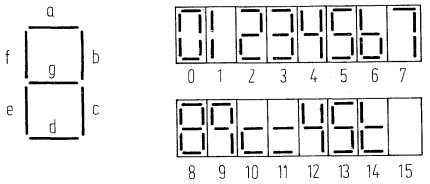
Electrical characteristics, 15 V range

Temperature range 1

Supply voltage	V_S		13.5	15	16.5	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}			4.5	V
L-output voltage for						
outputs a to g	V_{QL}	$I_{QL} = 20$ mA, $V_S = V_{SB}$		0.4	0.7	V
	V_{QL}	$I_{QL} = 40$ mA*), $V_S = V_{SB}$		0.7	1	V
output BI/RBQ	V_{QL}	$I_{QL} = 9$ mA			1.7	V
Output voltage for						
outputs a to g	V_Q	$V_S = V_{SB}$, $I_Q = 25\,\mu$A			16.5	V
H-output voltage at BI/RBQ	V_{QH}	$V_S = V_{SA}$, $-I_{QH} = 0.1$ mA	12	14.3		V
DC noise margin						
H-signal	V_{nm}		4.5	8		V
L-signal	V_{nm}		2.8	5		V
H-input current						
at A, B, C, D, RBI	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$			10	µA
at BI/RBQ	I_{IH}				20	µA
at LT	I_{IH}				30	µA
L-input current						
at A, B, C, D, RBI	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V		1.2	2.6	mA
at BI/RBQ	$-I_{IL}$			2.4	5.2	mA
at LT	$-I_{IL}$			3.6	7.8	mA
Supply current	I_S	$V_S = V_{SA}$, outputs open			44	mA

*) Duty cycle 1:1

Segment identification
Output patterns

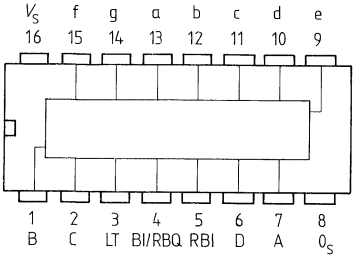


Truth table

Function	LT	RBI	D	C	B	A	BI/RBQ	a	b	c	d	e	f	g
0[1])	H	H	L	L	L	L	H	L	L	L	L	L	L	H
1	H	X	L	L	L	H	H	H	H	H	H	L	L	H
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L
11	H	X	H	L	H	H	H	H	H	H	L	H	H	L
12	H	X	H	H	L	L	H	H	L	L	H	H	L	L
13	H	X	H	H	L	H	H	L	H	L	L	H	L	L
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H
BI[2])	X	X	X	X	X	X	L	H	H	H	H	H	H	H
RBI[3])	H	L	L	L	L	L	L	H	H	H	H	H	H	H
LT[4])	L	X	X	X	X	X	H	L	L	L	L	L	L	L

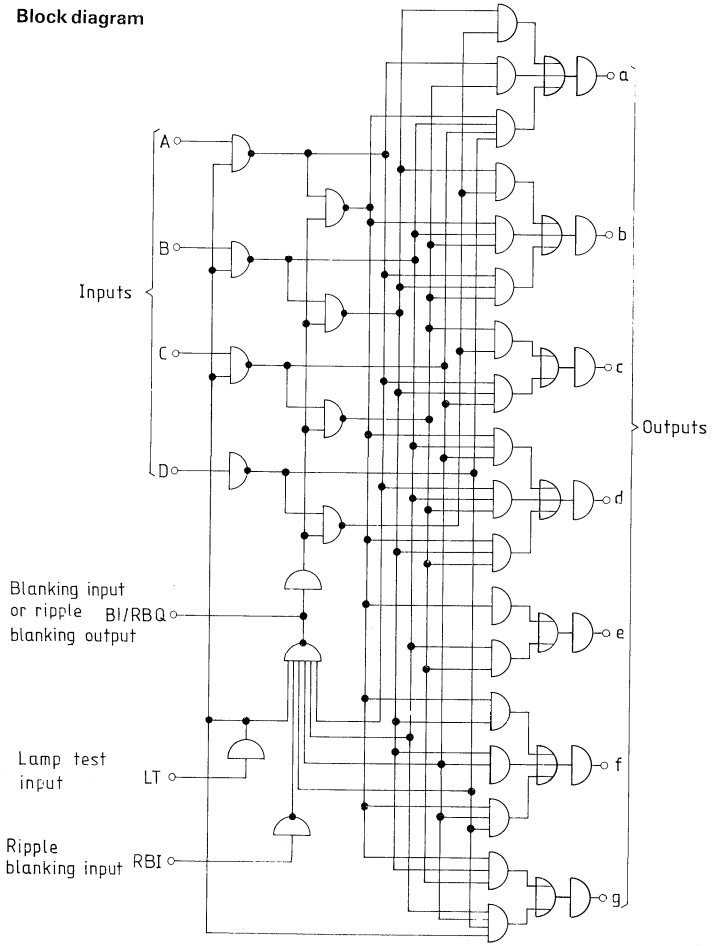
Notes:

X = H or L signal.
[1]) If 0-indication is desired, RBI must be supplied with an H-signal.
[2]) An L-signal at BI forces all segment outputs into H state independent of the other input conditions.
[3]) If an L-signal is supplied to RBI, H-signal results at all outputs and an L-signal at RBQ provided L-signal is applied to the inputs A, B, C, D (zero condition).
[4]) An L-signal at LT switches all outputs to L only if BI/RBQ is supplied with an H-signal regardless of the input condition at A, B, C, D, and RBI.



Pin configuration
top view

Block diagram



The integrated circuits FZL 121/125, S, FZL 131/135, S, and FZL 141/145, S are short-circuit proof power drivers for the following operating modes:

FZL 121/125: Driver with open collector output and 3 inputs for 20 V
FZL 131/135: Driver with open emitter output and 4 inputs for 20 V
FZL 141/145: Driver for power transistors for 20 V
FZL 121 S/125 S: Driver with open collector output and 3 inputs for 30 V
FZL 131 S/135 S: Driver with open emitter output and 4 inputs for 30 V
FUL 141 S/145 S: Driver for power transistors for 30 V

In the case of a short circuit, the load current is switched off and the circuit checks periodically with the aid of a built-in clock generator whether the short circuit is still present. The clock generator requires an external capacitor C_T between pin C and ground. Up to 8 clock terminals CLK of the types FZL 121/125, S, FZL 131/135, S, and FZL 141/145, S, can be connected in parallel, with only one capacitance on one integrated circuit. The C terminals of the remaining ICs must be connected to the supply voltage V_S.

In order to avoid oscillation in the case of a short circuit, a capacitive connection is necessary (C_{N1} and C_{N2} for FZL 121/125, S, FZL 131/135, S, and C for FZL 141/145, S). The typical values for C_{N1} and C_{N2} are suitable for line lengths $l < 50$ m. The values for C_{N1}, C_{N2} and C also determine the value of the load capacitance C_L. For resistive loading R_L, the range is restricted as shown in figure 1. In the prohibited region of this figure, the short-circuit protection does not react and there is a danger that the integrated circuits will be destroyed. In the case of a short circuit, transition through this region must be executed in approximately 50 ms.

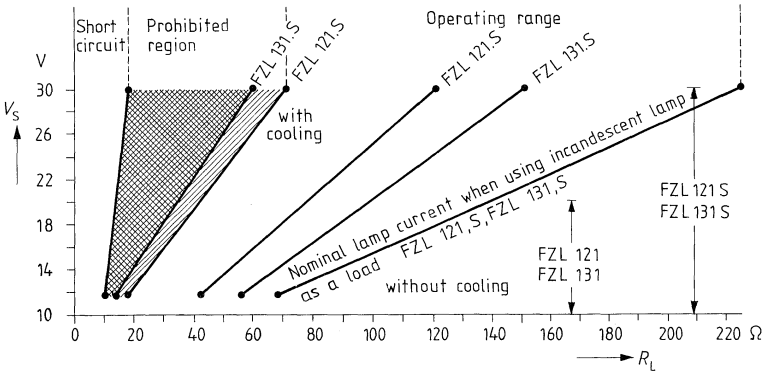


Figure 1
If the FZL circuits are driven by normalized LSL outputs, the output load factor is $F_{QH\,max} = 4$.

All functional inputs have Schmitt trigger characteristics. The circuits offer protection against short circuit and wire breakage, as the input currents must be positive, i.e. the circuits can be turned on only by an active H signal. This means that an open-circuit or short-circuit input corresponds to an L signal. Figure 2 shows the input circuit.

Overvoltage protection at the inputs:
With a series resistance of at least 4.7 kΩ connected to the input, the ICs are protected against interference voltages up to 150 V/50 µs with a duty cycle of 1 %. The cooling fins of types FZL 121/125 S and FZL 131/135 S may be connected to ground O_S. The thermal resistance of the heat sink used must have the following values:

R_{thH} = 50° C/W at I_Q = 175/200 mA, T_{amb} = 85° C
R_{thH} = 30° C/W at I_Q = 400 mA, t_{amb} = 70° C
R_{thH} = 15° C/W at I_Q = 400 mA, T_{amb} = 85° C

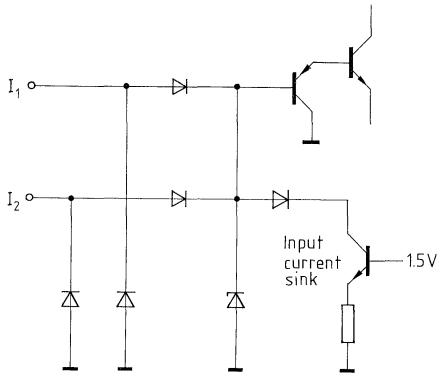


Figure 2
Input circuit

Type	Ordering code
FZL 121	Q67000-L168
FZL 125	Q67000-L174

The FZL 121 and FZL 125 are power stages for output currents up to 400 mA or nominal lamp currents up to 150 mA. The FZL 121 and FZL 125 have 3 NOR-gated inputs with Schmitt trigger characteristic. The load is connected between output Q and supply voltage V_S.

Electrical characteristics
Temperature range 1 and 5

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S		11.4	15	20	V
H-input voltage	V_{IH}	$V_S = V_{SA}$ to V_{SB}	8			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ to V_{SB}			6	V
Hysteresis	V_H	$V_S = V_{SA}$ to V_{SB}		0.4		V
L-output voltage	V_{QL}	$V_I = V_S$, $I_{QL} = 0.4$ A		1.5	2.2	V
Input current	I_{IL}	$0 < V_I < V_S$			250	µA
Output current[1])	I_{QL}	$T_{case} < 100°$ C			400	mA
	I_{QL}	$T_{amb} < 70°$ C			250	mA
	I_{QL}	$T_{amb} < 85°$ C			200	mA
for lamps	I_{QL}				150	mA
Short-circuit output current	I_Q	$R_L = 0$ to 15 Ω, $V_S = 20$ V	0.4	0.8	1.3	A
Supply current	I_S	$I_{QL} = 0$, $C_C = 33$ nF		8	12	mA
Capacitance at C	C_C		20	33	40	nF
Pulse interval ratio	P/P		1:80	1:60	1:50	
Capacitance at N	C_{N1}		50	500	2500	pF
	C_{N2}		0.5	1.8	10	nF
Load capacitance without operating short-circuit protection	C_L	C_N typ.		39	50	nF

[1]) Inductive loads must be provided with a quench diode.

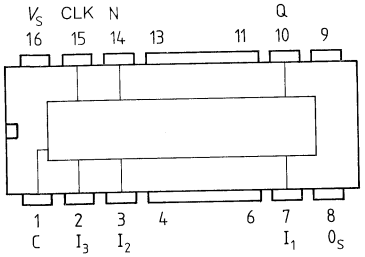
Type	Ordering code
FZL 121 S	Q67000-L168-S1
FZL 125 S	Q67000-L174-S1

The FZL 121 S and FZL 125 S are power stages for output currents up to 400 mA or nominal lamp currents up to 130 mA. The FZL 121 S and FZL 125 S have 3 NOR-gated inputs with Schmitt trigger characteristic. The load is connected between output Q and supply voltage V_S.

Electrical characteristics
Temperature range 1 and 5

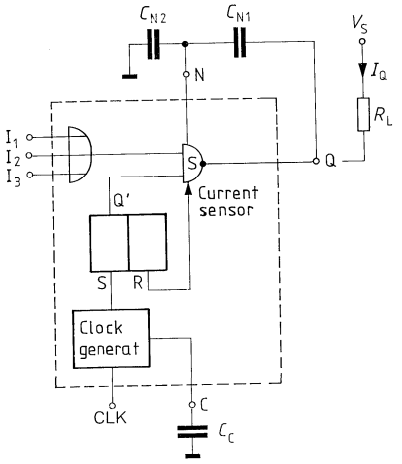
		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S		11.4	15	30	V
H-input voltage	V_{IH}	$V_S = V_{SA}$ to V_{SB}	8			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ to V_{SB}			6	V
Hysteresis	V_H	$V_S = V_{SA}$ to V_{SB}		0.4		V
L-output voltage	V_{QL}	$V_I = V_S$, $I_{QL} = 0.4$ A		1.5	2.2	V
Input current	I_I	$0 < V_I < V_S$			250	µA
Output current[1])	I_{QL}	$T_{case} < 100°C$			400	mA
	I_{QL}	$T_{amb} < 70°C$			250	mA
	I_{QL}	$T_{amb} < 85°C$			200	mA
for lamps	I_{QL}				150	mA
Short-circuit output current	I_Q	$R_L = 0$ to 22 Ω, $V_S = 30$ V	0.4	0.8	1.3	A
Supply current	I_S	$I_{QL} = 0$, $C_C = 33$ nF		8	12	mA
Capacitance at C	C_C		20	33	40	nF
Pulse interval ratio	P/P		1:80	1:60	1:50	
Capacitance at N	C_{N1}		50	500	2500	pF
	C_{N2}		0.5	1.8	10	nF
Load capacitance without operating short-circuit protection	C_L	C_N typ.		39	50	nF

[1]) Inductive loads must be provided with a quench diode.

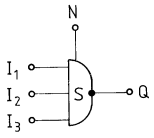


Pin configuration
top view
I_1, I_2, I_3 = Inputs
Q = Output
CLK = Clock output
C = Terminal for clock capacitance

Logic diagram for short-circuit operation



Logic diagram for normal operation (no short circuit)



Type	Ordering code
FZL 131	Q67000-L169
FZL 135	Q67000-L175

The FZL 131 and FZL 135 are power stages for output currents up to 400 mA, or for nominal lamp currents up to 150 mA. The FZL 131 and FZL 135 have 4 OR-gated inputs with Schmitt trigger characteristic. The load is connected between output Q and ground O_S.

Electrical characteristics

Temperature range 1 and 5

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S		11.4	15	20	V
H-input voltage	V_{IH}	$V_S = V_{SA}$ to V_{SB}	8			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ to V_{SB}			6	V
Hysteresis	V_H	$V_S = V_{SA}$ to V_{SB}		0.4		V
H-output voltage	V_{QH}	$-I_{QL} = 0.4$ A	$V_S - 2.7$	$V_S - 2$		V
Input current	I_I	$0 < V_I < V_S$			250	µA
Output current[1])	$-I_{QH}$	$T_{case} < 100°C$			400	mA
	$-I_{QH}$	$T_{amb} < 70°C$			200	mA
	$-I_{QH}$	$T_{amb} < 85°C$			175	mA
for lamps	$-I_{QH}$				150	mA
Short-circuit output current	$-I_Q$	$R_L = 0$ to $15\,\Omega$, $V_S = 20$ V	0.4	0.8	1.3	A
Supply current	I_S	$I_{QH} = 0$, $C_C = 33$ nF		7	11	mA
Capacitance at C	C_C		20	33	40	nF
Pulse interval ratio	P/P		1:80	1:60	1:50	
Capacitance at N	C_{N1}		50	500	2500	pF
	C_{N2}		0.5	1.8	10	nF
Load capacitance without operating short-circuit protection	C_L	C_N typ.		39	50	nF

[1]) Inductive loads must be provided with a quench diode.

Type	Ordering code
FZL 131 S	Q67000–L169-S1
FZL 135 S	Q67000–L175-S1

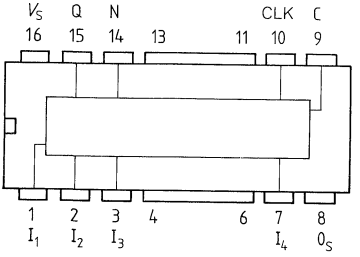
The FZL 131 S and FZL 135 S are power stages for output currents up to 400 mA or nominal lamp currents up to 130 mA. The FZL 131 S and FZL 135 S have 4 OR-gated inputs with Schmitt trigger characteristic. The load is connected between output Q and ground O_S.

Electrical characteristics

Temperature range 1 and 5

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S		11.4	15	30	V
H-input voltage	V_{IH}	$V_S = V_{SA}$ to V_{SB}	8			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ to V_{SB}			6	V
Hysteresis	V_H	$V_S = V_{SA}$ to V_{SB}		0.4		V
H-output voltage	V_{QH}	$-I_Q = 0.4$ A	$V_S-2.7$	V_S-2		V
Input current	I_I	$0 < V_I < V_S$			250	µA
Output current[1])	$-I_{QH}$	$T_{case} < 100°C$			400	mA
	$-I_{QH}$	$T_{amb} < 70°C$			200	mA
	$-I_{QH}$	$T_{amb} < 85°C$			175	mA
for lamps	$-I_{QH}$				130	mA
Short-circuit output current	$-I_Q$	$R_L = 0$ to $22\,\Omega$, $V_S = 30$ V	0.4	0.8	1.3	A
Supply current	I_S	$I_{QH} = 0$, $C_C = 33$ nF		7	11	mA
Capacitance at C	C_C		20	33	40	nF
Pulse interval ratio	P/P		1:80	1:60	1:50	
Capacitance at N	C_{N1}		50	500	2500	pF
	C_{N2}		0.5	1.8	10	nF
Load capacitance without operating short-circuit protection	C_L	C_N typ.		39	50	nF

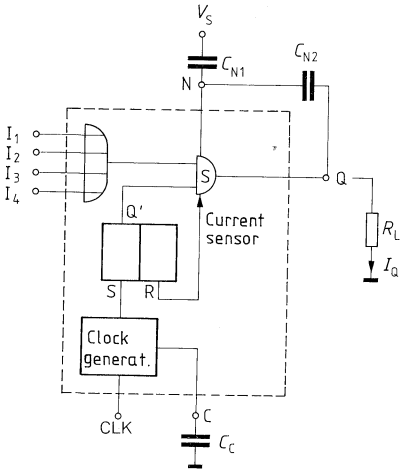
[1]) Inductive loads must be provided with a quench diode.



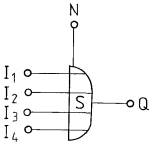
Pin configuration
top view

I_1, I_2, I_3, I_4 = Inputs
Q = Output
CLK = Clock output
C = Terminal for clock capacitance

Logic diagram for short-circuit operation



Logic diagram for normal operation (no short circuit)



Type	Ordering code
FZL 141	Q67000-L170
FZL 145	Q67000-L176

The FZL 141 and FZL 145 are drivers for transistor power stages with high output currents. The controlled power stage ist short-circuit protected. The FZL 141 and FZL 145 have an input with Schmitt trigger characteristic.

Electrical characteristics
Temperature range 1 and 5

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S		11.4	15	20	V
H-input voltage	V_{IH}	$V_S = V_{SA}$ to V_{SB}	8			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ to V_{SB}			6	V
Hysteresis	V_H	$V_S = V_{SA}$ to V_{SB}		0.4		V
Voltage at base T_1	V_X	$5\,mA < I_X < 25\,mA$	$V_S - 2$	$V_S - 2.2$	$V_S - 2.4$	V
Turn-off voltage for overload	V_W		$V_S - 0.7$	$V_S - 0.8$	$V_S - 0.9$	V
Input current lower limit at 20° C	I_I	$0 < V_I < V_S$			250	µA
Current at X	$-I_X$				25	mA
Output current at Q	I_Q				25	mA
Supply current	I_S	$V_I = V_S$, $I_Q = 25\,mA$, $C_C = 33\,nF$		6	10	mA
Capacitance at C	C_C		20	33	40	nF
Pulse interval ratio	P/P		1:80	1:60	1:50	

Electrical characteristics of the recommended circuit

Recommended power transistors: one stage: T_1 = BD 136-10
two stages: T_1 = BSV 15-10, T_2 = 2N 3055
one Darlington stage: T_3 = BD 676

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Output voltage	V_{Q1}	with BD 136, $I_{Q1} = 0.5$ A	$V_S - 1.8$	$V_S - 1$		V
	V_{Q2}	with BSV 15 and 2 N 3055 or BD 676, $I_{Q2} = 3$ A	$V_S - 3.2$	$V_S - 2$		V
Output current	I_{Q1}	with BD 136, $R_C = 1.3\,\Omega$			0.5	A
for lamps	P_{Q1}				1	W
Output current	I_{Q2}	with BSV 15 and 2 N 3055 or BD 676, $R_C = 0.22\,\Omega$			3	A
for lamps	P_{Q2}				8.5	W
Resistance	R_V		$\frac{V_S - 1}{I_{Q\max}}$			V/A
	R_C		$\frac{V_W}{I_{Q1} + I_{Q2}}$			V/A
	R_B			47		Ω

Type	Ordering code
FZL 141 S	Q67000–L170-S1
FZL 145 S	Q67000–L176-S1

The FZL 141 S and FZL 145 S are drivers for transistor power stages with high output currents. The controlled power stage is short-circuit protected. The FZL 141 S and FZL 145 S have an input with Schmitt trigger characteristic.

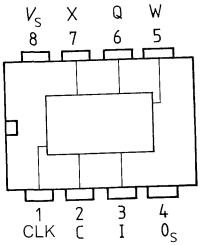
Electrical characteristics
Temperature range 1 and 5

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S		11.4	15	30	V
H-input voltage	V_{IH}	$V_S = V_{SA}$ to V_{SB}	8			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ to V_{SB}			6	V
Hysteresis	V_H	$V_S = V_{SA}$ to V_{SB}		0.4		V
Voltage at base T_1	V_X	$5\,mA < I_X < 25\,mA$	V_S-2	$V_S-2.2$	$V_S-2.4$	V
Turn-off voltage for overload	V_W		$V_S-0.7$	$V_S-0.8$	$V_S-0.9$	V
Input current at I	I_I	$0 < V_I < V_S$			250	µA
Current at X	$-I_X$				25	mA
Output current at Q	I_Q				25	mA
Supply current	I_S	$V_I = V_S$, $I_Q = 25\,mA$, $C_C = 33\,nF$		6	10	mA
Capacitance at C	C_C		20	33	40	nF
Pulse interval ratio	P/P		1:80	1:60	1:50	

Electrical characteristics of the recommended circuit

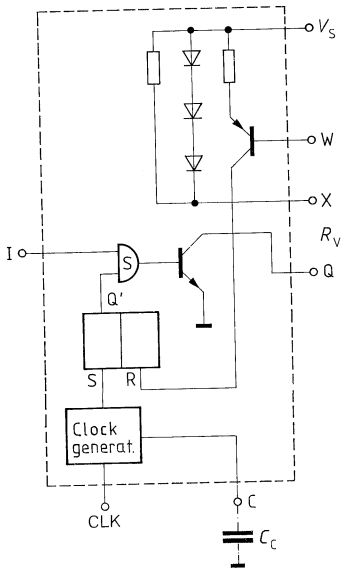
Recommended power transistors: one stage: T_1 = BD 136-10
two stages: T_1 = BSV 15-10, T_2 = 2N 3055
one Darlington stage: T_3 = BD 676

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Output voltage	V_{Q1}	with BD 136, $I_{Q1} = 0.5$ A	$V_S - 2.0$	$V_S - 1$		V
	V_{Q2}	with BSV 15 and 2 N 3055 or BD 676, $I_{Q2} = 3$ A	$V_S - 4.0$	$V_S - 2$		V
Output current for lamps	I_{Q1}	with BD 136, $R_C = 1.3\,\Omega$			0.5	A
	P_{Q1}				1	W
Output current for lamps	I_{Q2}	with BSV 15 and 2 N 3055 or BD 676, $R_C = 0.22\,\Omega$			3	A
	P_{Q2}				8.5	W
Resistors	R_V		$\frac{V_S - 1}{I_{Qmax}}$			V/A
	R_C		$\frac{V_W}{I_{Q1} + I_{Q2}}$			V/A
	R_B			47		Ω

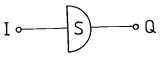


Pin configuration
top view
I = Input
Q = Output
CLK = Clock output
C = Terminal for clock capacitance
X, W = Inputs for short-circuit protection

Logic diagram for short-circuit operation



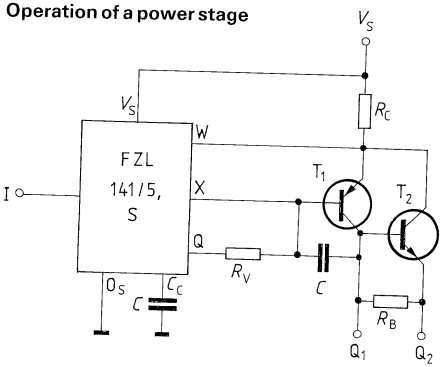
Logic diagram for normal operation (no short circuit)



Typical applications

The load conditions at Q, Q_1, and Q_2 are determined by the maximum power dissipation of the power transistors. In particular, the pulsed power dissipation during short-circuit operation has to be observed.

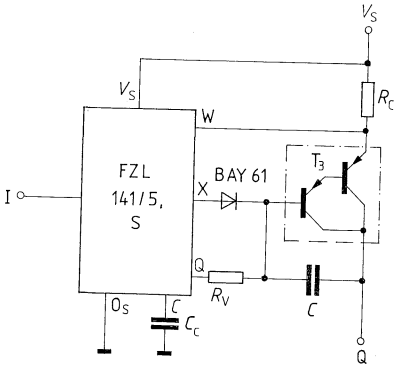
Operation of a power stage



Delayed response of short-circuit protection

The short-circuit protection can be delayed by an RC network connected to W and V_S, in order to avoid response when large load capacitors C_L are used. The maximum permissible resistance $R = 1\ k\Omega$. The maximum permissible power dissipation of the driven transistor determines the value of capacitor C.

Operation of a power Darlington stage



Type	Ordering code
FZY 101	Q67000-Y361
FZY 105	Q67000-Y362

The ICs FZY 101 and FZY 105 contain two constant voltage sources. Voltage source 1 can be set to an output voltage of 12 V, 13 V, 14 V, 15 V, or 17 V. The permissible load current is 120 mA, but this range can be extended with the aid of a power transistor. The collector of the power transistor is connected to V_{S1}, the base to V_1, and the emitter to X, Y, or Z_1, depending on the required output voltage. The output voltage is then taken from the emitter.
Voltage source 2 can be set to an output voltage of 12 V or 17 V, with load currents up to 25 mA. It can be extended for higher currents only in the 12 V range.
Both voltage sources can be set to different output voltage values in the range 12 V to $V_S - 2$ V by connection of external parallel resistors. In order to avoid self-oscillation caused, for example, by long leads, a capacitor with a value of 0.1 to 1 µF should be connected between V_S and O_S.
The heat must be dissipated by the cooling fins (pins 4/6, 12/13). These cooling fins may be connected to ground.
Both voltage sources are connected only to ground pin O_S and can thus be operated independently with different output voltages (V_{S1}, V_{S2}).

Maximum ratings

		Upper limit A	Unit
Power dissipation	P_{tot}	0.7	W
Junction temperature	T_j	125	°C
Thermal resistance	$R_{thjcase}$	20	°C/W

Electrical characteristics

Temperature range 1 and 5

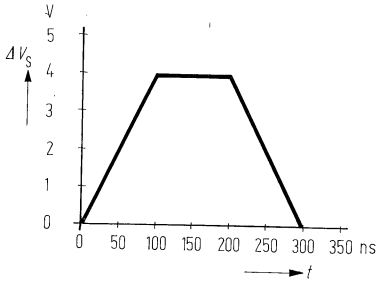
		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
1st voltage source						
Supply voltage	V_{S1}		0		30	V
Supply current	I_S	V_1 and X connected, $I_L = 0$		3.7	5.5	mA
Output voltage	V_1	V_1 and Z_1 connected, $V_{S1} \geq 15$ V, $-I_L \leq 120$ mA	11.2	12	12.8	V
Output voltage	V_1	V_1, Y and X, Z_1 connected, $V_{S1} \geq 16$ V, $-I_L \leq 120$ mA		13		V
Output voltage	V_1	V_1, X and Y, Z_1 connected, $V_{S1} \geq 17$ V, $-I_L \leq 120$ mA		14		V
Output voltage	V_1	V_1 and Y connected, $V_{S1} \geq 18$ V, $-I_L \leq 120$ mA	14.1	15	15.9	V
Output voltage	V_1	V_1 and X connected, $V_{S1} \geq 20$ V, $-I_L \leq 120$ mA	16	17	18	V
Load current	I_L				120	mA

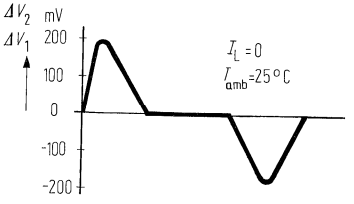
Electrical characteristics

Temperature range 1 and 5

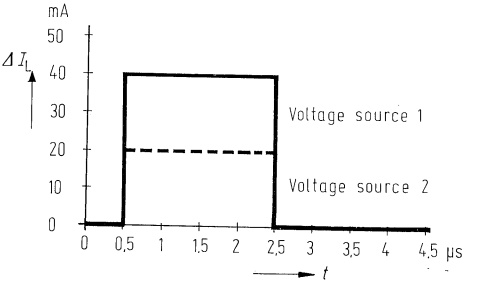
		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
2nd voltage source						
Supply voltage	V_{S2}		0		30	V
Supply current	I_S	$I_L = 0$		3.7	5.5	mA
Output voltage	V_2	V_2 and Z_2 connected $V_{S2} \geqq 15\,V, -I_L \leqq 25\,mA$	11.2	12	12.8	V
Output voltage	V_2	$V_{S2} \geqq 20\,V, -I_L \leqq 25\,mA$	16	17	18	V
Load current	I_L				25	mA
Voltage difference between V_1 and V_2	ΔV	$I_{L1} = 45\,mA$ | V_1 and X connected $I_{L2} = 15\,mA$ |			0.5	V

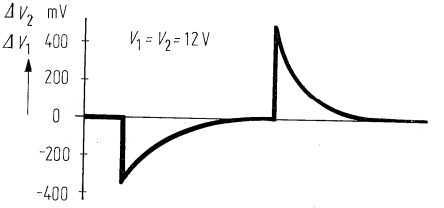
Input voltage variation

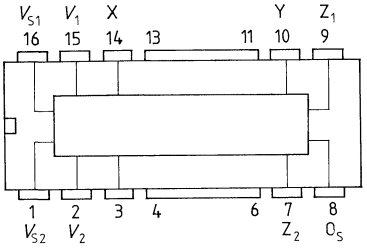




Load variation



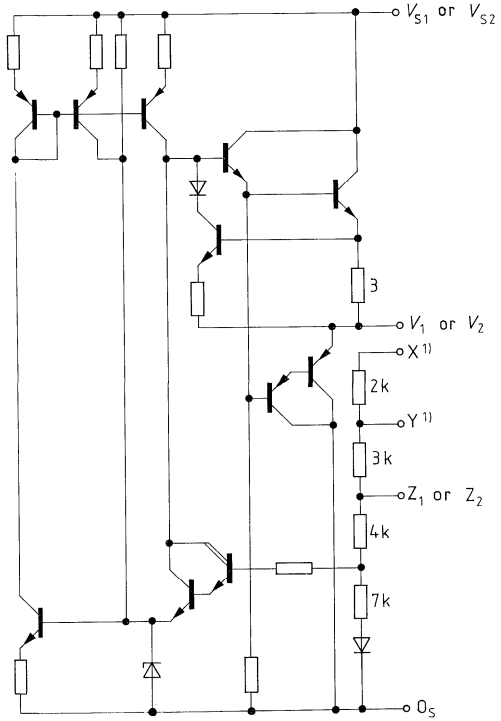




Pin configuration
top view

X, Y, Z = Terminals for voltage adjustment
V_1, V_2 = Outputs

Block diagram (one supply circuit)



1) X, Y in circuit 1 only. In circuit 2, X is connected internally to output V_2.

Type	Ordering code
S 353	Q67000–R109

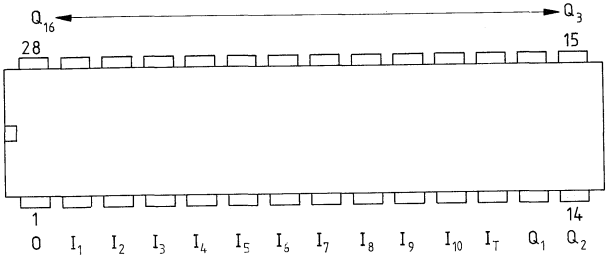
The IC S 353 is a programmable diode matrix with 10 inputs and 16 outputs. The substrate potential (O) must be equal or negative referred to that at the inputs.

Electrical characteristics of the single diodes, including fuse

($T_{amb} = 25°C$)

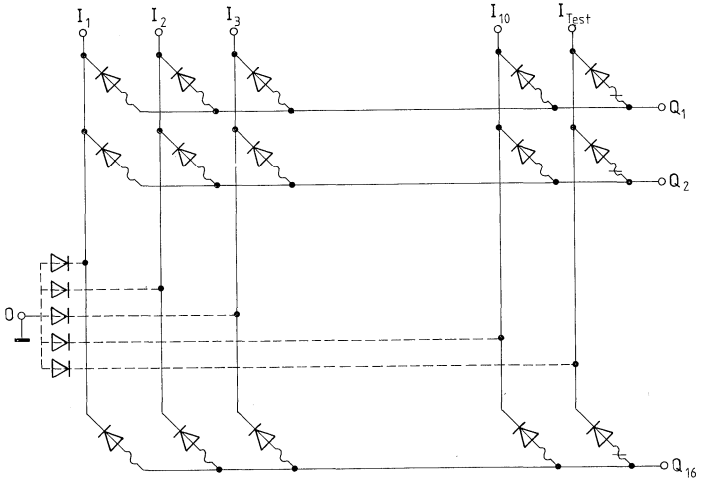
		Test conditions	Lower limit B	Upper limit A	Unit
Reverse voltage	V_R	$I_R = 100\,\mu A$	20		V
Forward voltage	V_F	$I_F = 1\,mA$		1.5	V
Reverse current[1])	I_R	$V_R = 10\,V$		10	nA
Capacitance between input and output	C	$V_R = 10\,V$		8	pF
Programming current	I_Q	Pin O $= -2\,V$, $V_I = 0\,V$		50	mA
Resistance of the programmed diode path	R		1		MΩ

[1]) Reverse current aimed at the output when all diodes are present, at an input voltage $V_I = 10$ V and an output voltage $V_Q = 9.5$ V: $I_R < 10\,\mu A$.



Pin configuration
top view

Circuit

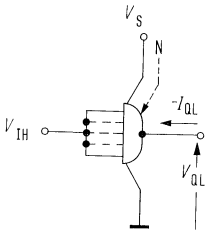


Note: Inputs must not be open
$V_I < V_Q$

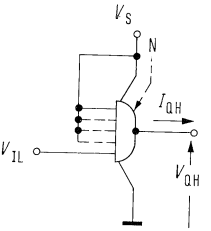
Programming conditions

1. Pin O (substrate) must be 2 V more negative than ground (corresponding input I).
2. Apply the programming current of 45 to 50 mA, with a duration of 5 to 10 ms, to the appropriate output Q.
3. Normally, one pulse is sufficient for programming.

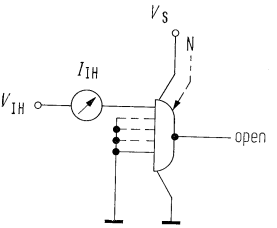
The test circuits are shown for NAND gates. They apply similarly to gates with other functions.



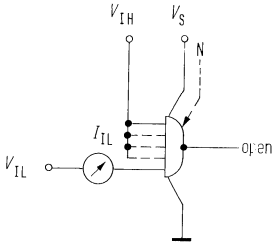
Test circuit 1



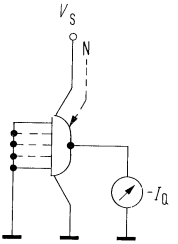
Test circuit 2



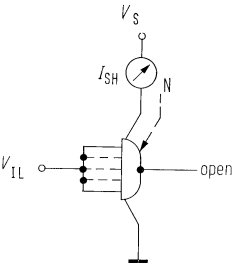
Test circuit 3



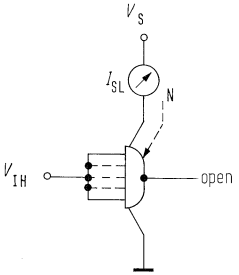
Test circuit 4



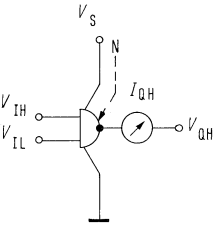
Test circuit 5



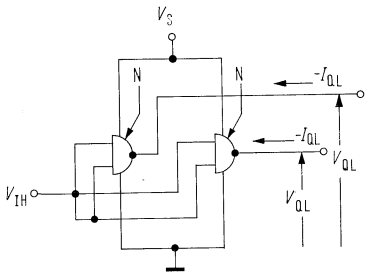
Test circuit 6



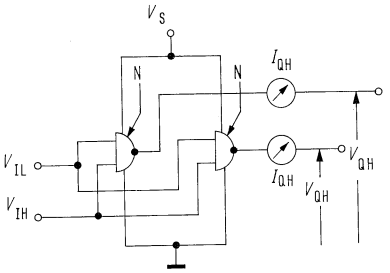
Test circuit 7



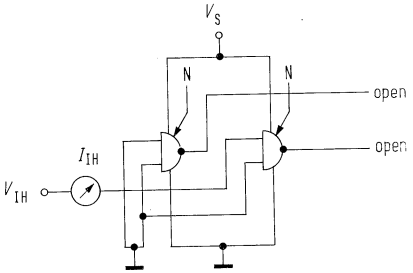
Test circuit 8



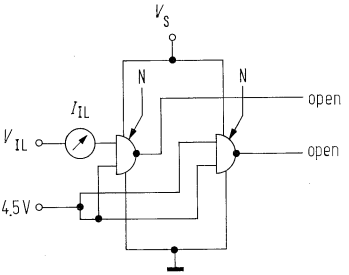
Test circuit 9



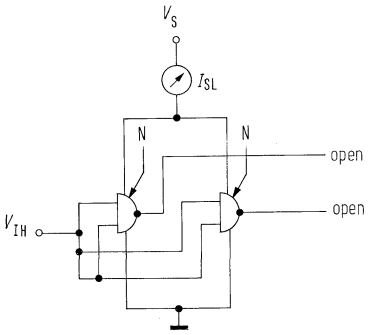
Test circuit 10



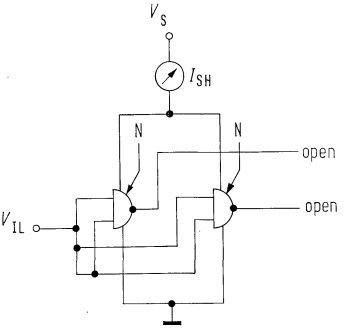
Test circuit 11



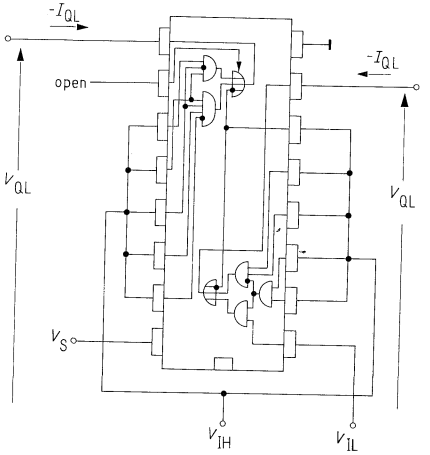
Test circuit 12



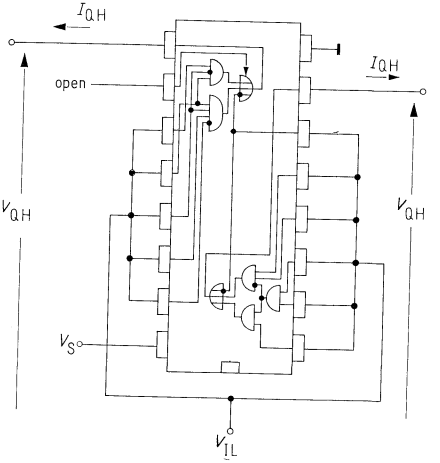
Test circuit 13



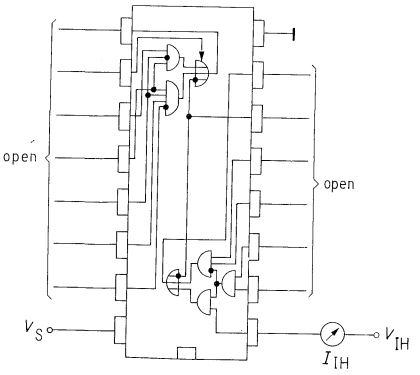
Test circuit 14



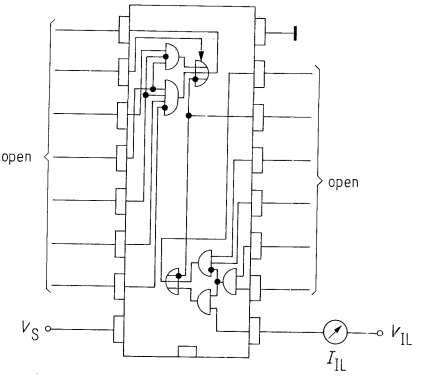
Test circuit 15



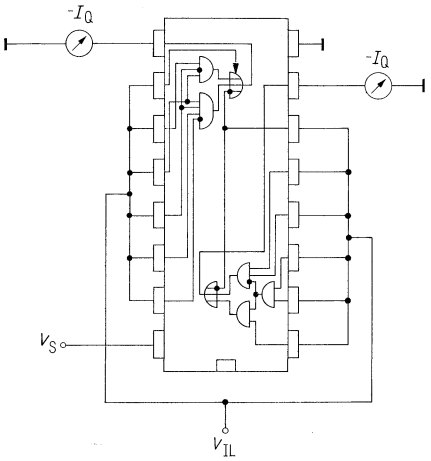
Test circuit 16



Test circuit 17

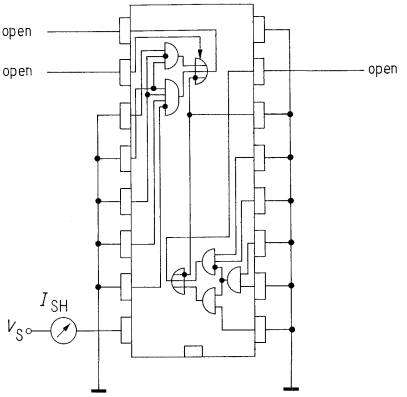


Test circuit 18

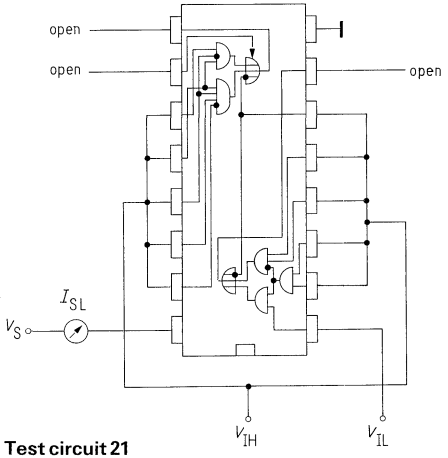


Each output is tested separately

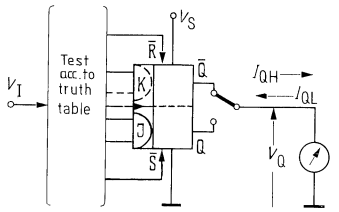
Test circuit 19



Test circuit 20



Test circuit 21

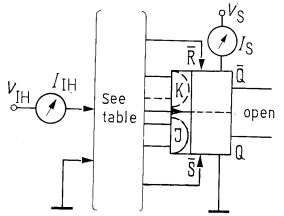


Test circuit 22

Each output is tested separately

I_{IH}: each input is tested separately
I_S: V_{IH} is applied to all inputs

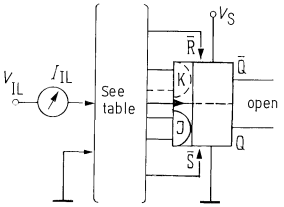
V_{IH} at	Ground at
J_1 or J_2	CLK, $\overline{S}$, J_1, or J_2
K_1 or K_2	CLK, R, K_1, or K_2
$\overline{R}$	CLK, J_1, and J_2
$\overline{S}$	CLK, K_1, and K_2
CLK	J_1, J_2, K_1, K_2, $\overline{R}$, $\overline{S}$



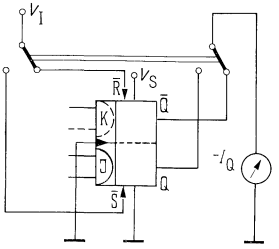
Test circuit 23

Each input is tested separately

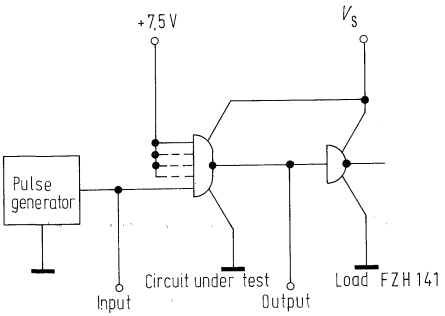
V_{IL} at	4.5 V at	17 V at
J_1, or J_2	$\overline{R}$	CLK, J_1, or J_2
K_1, or K_2	$\overline{S}$	CLK, K_1, or K_2
$\overline{R}$		J_1 and J_2
$\overline{S}$		K_1 and K_2
CLK		J_1, J_2, K_1, K_2

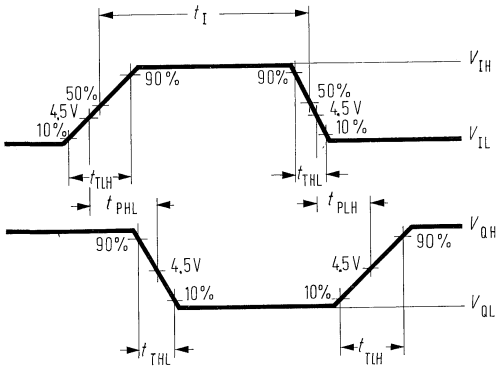


Test circuit 24



Test circuit 25

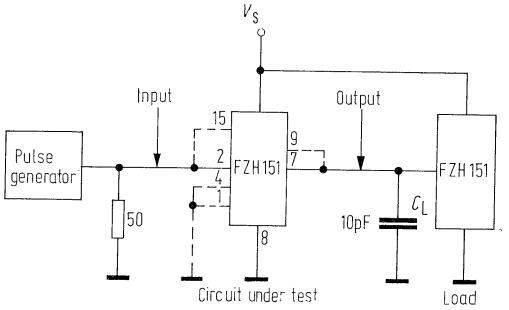


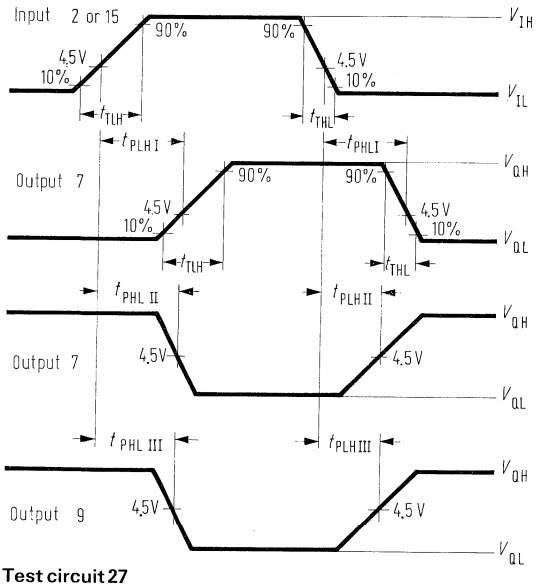


Test circuit 26

Pulse generator characteristic data: $t_{TLH} = 350$ ns, $t_{THL} = 120$ ns, $t_p = 1$ µs, pulse amplitude: +10 V.

The load consists of the circuit and leakage capacitances and one FZH 141 logic gate.

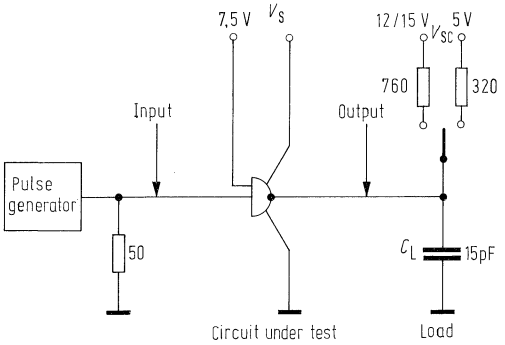


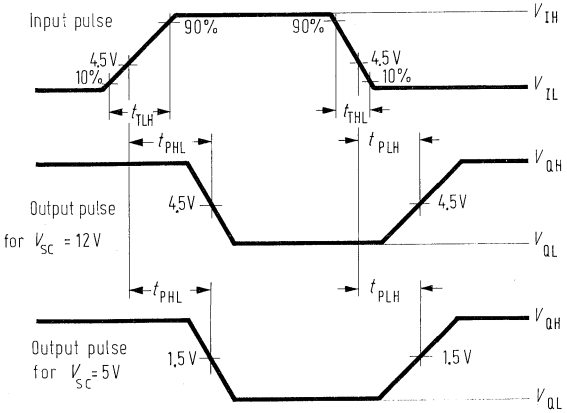


Test circuit 27

Pulse generator characteristic data: $t_{TLH} = 350$ ns, $t_{THL} = 240$ ns, pulse amplitude: $+10$ V.

For the measurement from input 2 to output 7, input 4 is connected to ground; input 1 being connected to ground for the second measurement. For measurement of input 15 to output 9, all other inputs remain open and t_{TLH} and t_{THL} are measured at the non-inverting output 7.

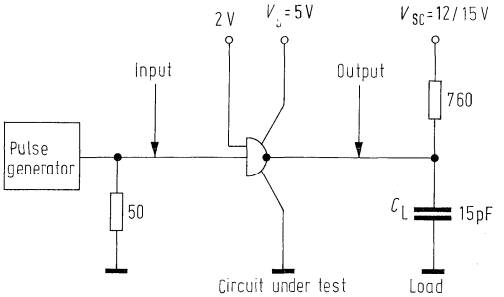


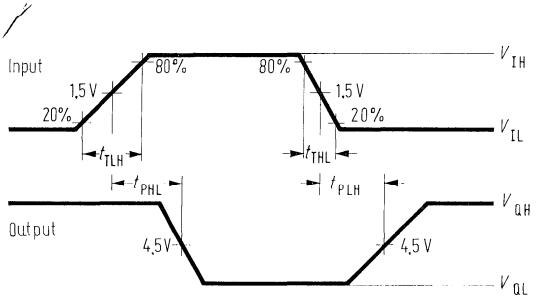


Test circuit 28

Pulse generator characteristic data: $t_{TLH} = 350$ ns, $t_{THL} = 120$ ns, pulse amplitude: +10 V.

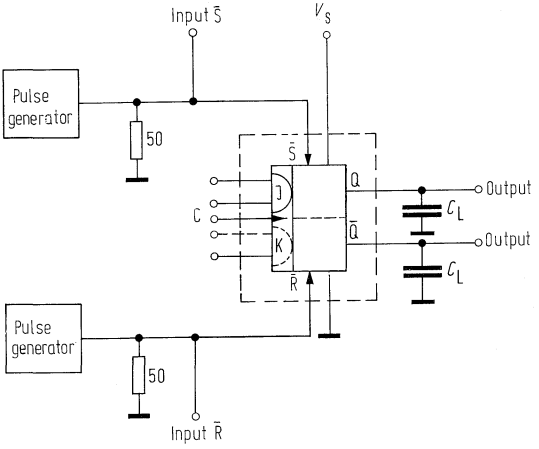
Measuring level: Input pulse 4.5 V above ground, output pulse 1.5 V (for $V_{SC} = 5$ V) or 4.5 V (for $V_{SC} = 12$ V) above ground.



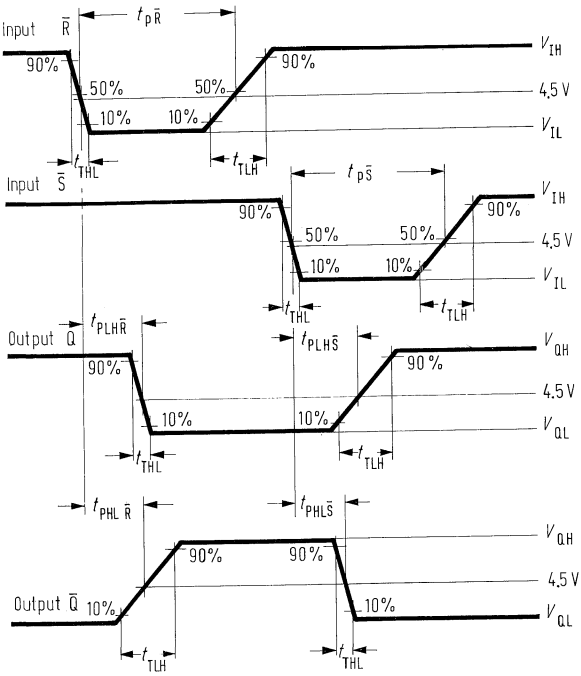


Test circuit 29

Pulse generator characteristic data: $t_{TLH} = 10$ ns, $t_{THL} = 5$ ns, pulse amplitude: + 3 V.
Measuring levels: 1.5 V above ground (input pulse), 4.5 V above ground (output pulse).



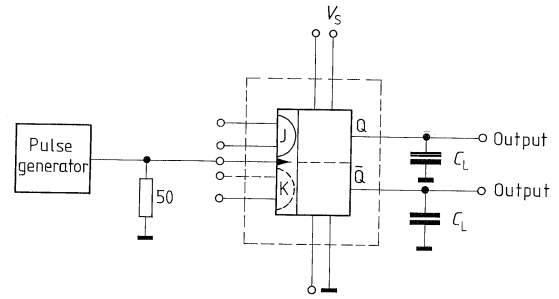
Measuring the delay time from $\overline{R}$ or $\overline{S}$ to Q or $\overline{Q}$

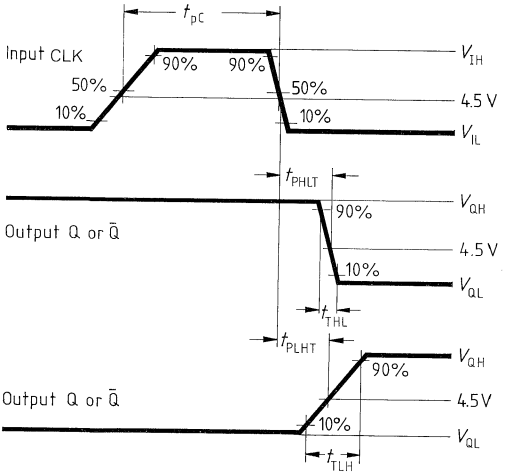


Pulse generator characteristic data:
$t_{THL} = 350$ ns,
$t_{TLH} = 120$ ns,
$t_{pR} = t_{pS} = 700$ ns,
pulse amplitude: +10 V.
Unused inputs are to be left open.
The load (C_L = 10 pF) includes the probe and added capacitances.
$t_{PHLR(S)}$ and $t_{PLHR(S)}$ are measured at a voltage of 4.5 V above ground.

Test circuit 30

Measuring the delay time "Clock to Q or $\overline{Q}$"

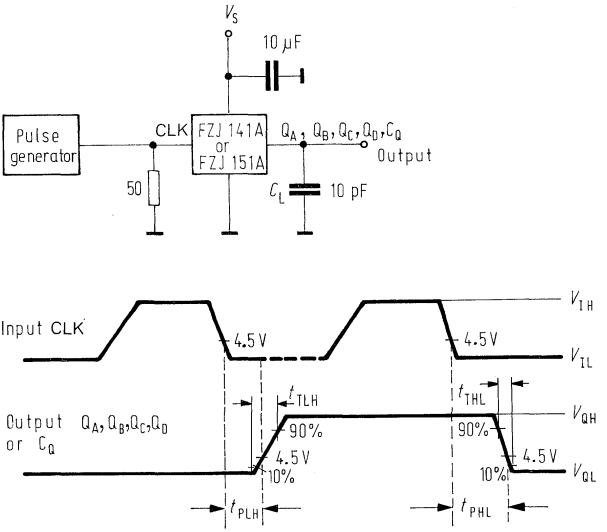




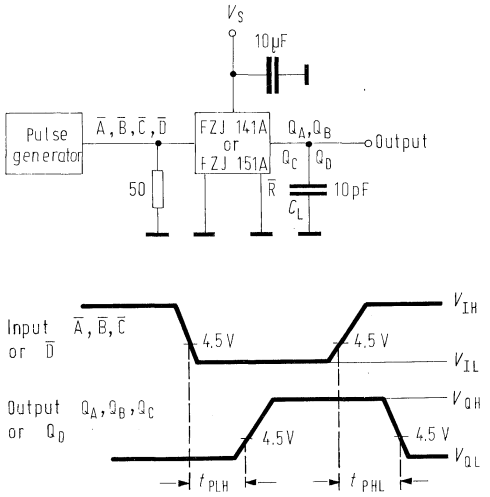
Test circuit 31

Pulse generator characteristic data: $t_{TLH} = 350$ ns, $t_{THL} = 120$ ns, $t_{pC} = 400$ ns.

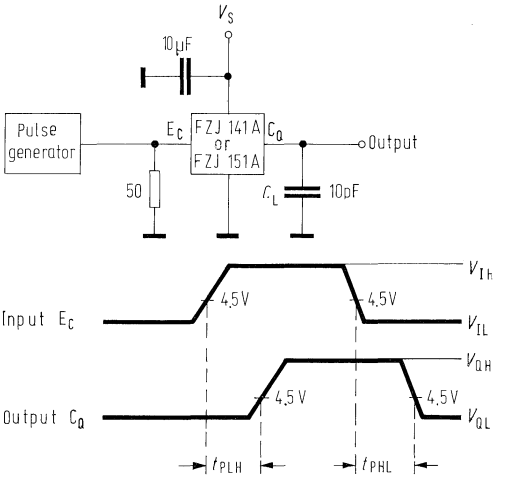
Pulse amplitude: +9 V, +1 V offset.
Unused inputs are to be left open.
The load ($C_L = 10$ pF) includes the probe and added capacitances.
t_{PHLT} and t_{PLHT} are measured at 4.5 V above ground.



Test circuit 50
Connect unused inputs to V_S.
The load C_L includes the probe and added capacitances.

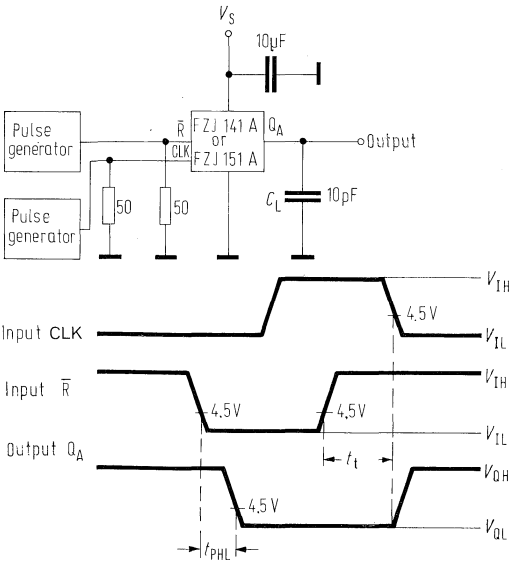


Test circuit 51
Connect unused inputs to V_S.

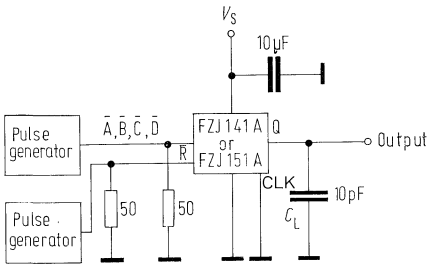


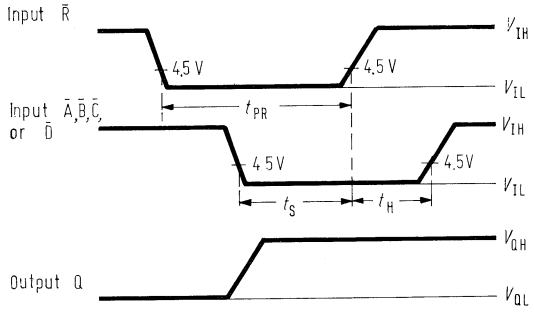
	Inputs						Output
	$\overline{A}$	$\overline{B}$	$\overline{C}$	$\overline{D}$	$\overline{R}$	CLK	C_Q
FZJ 141 A	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{QH}
FZJ 151 A	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{QH}

Test circuit 52
The load C_L includes the probe and added capacitances.



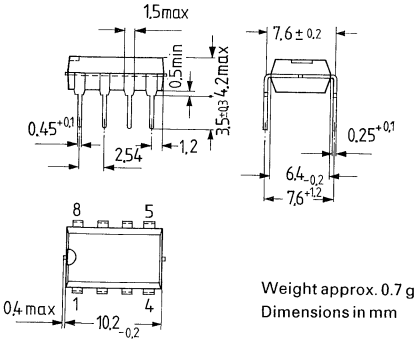
Test circuit 53
Connect unused inputs to V_S.





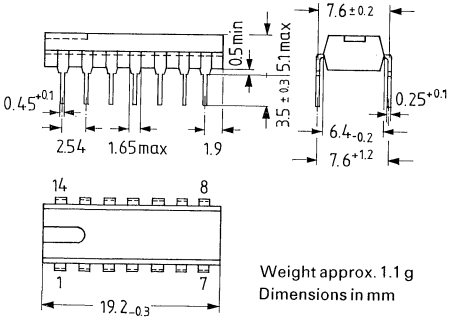
Test circuit 54
Connect unused inputs to V_S.
The load C_L includes the probe and added capacitances.

Plastic plug-in package, 8 pins, 20 A 8 DIN 41866



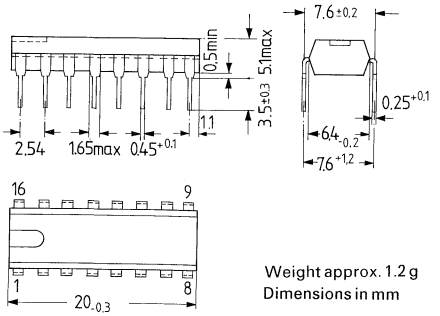
Weight approx. 0.7 g
Dimensions in mm

Plastic plug-in package, 14 pins, 20 A 14 DIN 41866



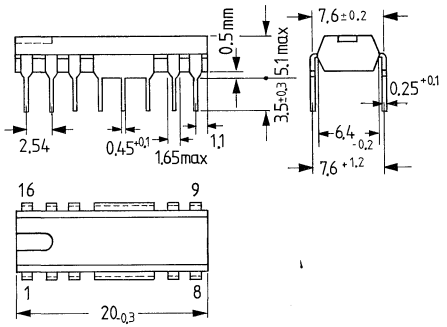
Weight approx. 1.1 g
Dimensions in mm

Plastic plug-in package, 16 pins, 20 A 16 DIN 41866



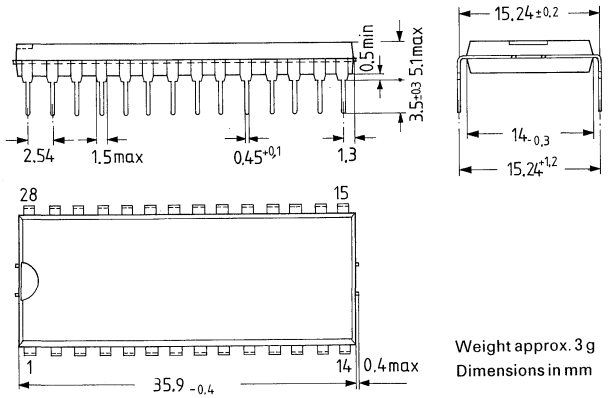
Weight approx. 1.2 g
Dimensions in mm

Plastic plug-in package, 16 pins, for power applications, 20 A 16 DIN 41866 (TO-116)



Weight approx. 1.1 g
Dimensions in mm

Plastic plug-in package, 28 pins, 20 A 28 DIN 41866



Weight approx. 3 g
Dimensions in mm

Hall Circuits

The ICs SAS 221, SAS 241, SAS 251, SAS 261 are magnetically operated contactless switches with the following operating modes:

	Supply voltage range	Function
SAS 221 S2 SAS 221 S4	10 to 27 V 4.75 to 18 V	Switch; static antivalent outputs with open collectors
SAS 241 SAS 241 S4	4.75 to 18 V 4.75 to 5.25 V	Switch; dynamic open collector outputs
SAS 251 SAS 251 S4 SAS 251 S5	4.75 to 27 V 4.75 to 5.25 V 4.75 to 18 V	Switch; static open collector outputs
SAS 261 SAS 261 S4	4.75 to 18 V 4.75 to 5.25 V	Switch; static open collector output and enable input

All ICs are available in a four-pin flat package. SAS 241 and SAS 251 are also available upon request as film-mounted version in a micropack.

The IC SAS 231L supplies a voltage proportional to the magnetic induction. Due to its micropack design, it is particularly suitable for operation in very small air gaps.

SAS 231L	4.75 to 15 V	Hall IC with output voltage proportional to magnetic field

Type	Ordering code
SAS 221 S2	Q67000-S33-S2
SAS 221 S4	Q67000-S33-S4

The ICs SAS 221 S2 and SAS 221 S4 are contactless switches, which are operated by a magnetic field. The outputs with open collectors permit wired AND operation for generation of encoded signals. The output Q changes from H to L at $B > B_{ON}$. The outputs Q and $\overline{Q}$ are always antivalent. The south pole of the magnetic field must always act vertically upon the surface marked with the notch.

Maximum ratings

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage						
SAS 221 S2	V_S		–0.5		30	V
SAS 221 S4	V_S		–0.5		20	V
Output current	I_Q, $I_{\overline{Q}}$				30	mA
Junction temperature	T_j				150	°C
Thermal resistance	R_{thsamb}				170	K/W
Storage temperature	T_s		–40		125	°C

Range of operation

Supply voltage						
SAS 221 S2	V_S		10		27	V
SAS 221 S4	V_S		4.75		18	V
Ambient temperature	T_{amb}		5		60	°C

Electrical characteristics at 18 V, T_{amb} = 5 to 60° C

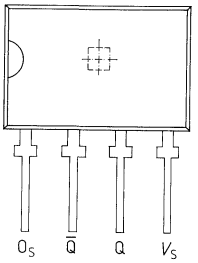
Supply current	I_S		3		7	mA
Flux density for "ON"	B_{ON}				0.065	T
Flux density for "OFF"	B_{OFF}		0.005			T
Maximum temperature deviation referred to 25° C	$\Delta B_{ON}/B_{OFF}$		–0.015		0.015	T
Hysteresis	B_{Hy}			0.015		0.035
Output leakage current	I_{Qlk}	$B < B_{OFF}$			10	µA
	$I_{\overline{Q}}$	$B > B_{ON}$			10	µA
Output voltage	V_Q, $V_{\overline{Q}}$	I_Q or $I_{\overline{Q}}$ = 16 mA			0.4	V

Delay times

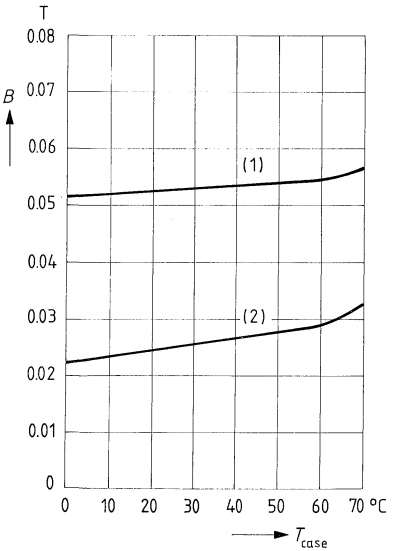
(V_S = 18 V, T_{amb} = 25° C)

Transition time	t_{THL}	between 90 and 10%			1	µs
	t_{TLH}	between 10 and 90%			2	µs

Pin configuration



Typical flux density for "ON" (1) and "OFF" (2) versus case temperature



Hall IC
with Output Voltage Proportional to Magnetic Field

SAS 231 L

Preliminary data

Type	Ordering code
SAS 231 L	Q67000–A1468-L

The IC SAS 231 L generates an output voltage proportional to the magnetic flux density. The output voltage increases when the south pole of a magnet approaches the top surface of the chip. The zero point is adjusted by external components. The steepness of the characteristic curve $V_Q = f(B)$ can be varied by external components.

Maximum ratings

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S		0		18	V
Output current	I_Q				10	mA
Storage temperature	T_s		–40		125	°C

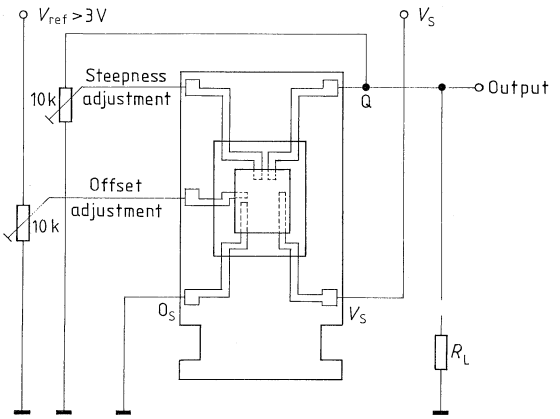
Range of operation

Supply voltage	V_S		4.75		15	V
Output current	I_Q				5	mA
Ambient temperature	T_{amb}		0		70	°C

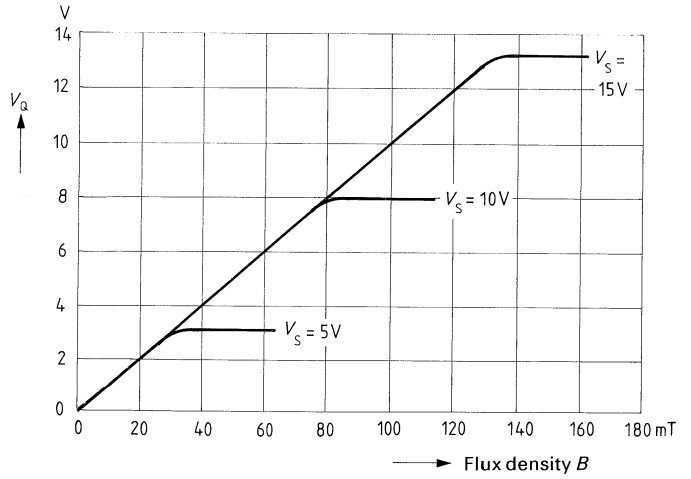
Electrical characteristics at $V_S = 10\,V$, $T_{amb} = 25°C$, unless otherwise specified

Supply current (no load)	I_S	$R_L = \infty$		6	10	mA
Output voltage	V_Q	$R_L = 10\,k\Omega$	0.05		V_S–2	V
Steepness (without adjustment)	S		60	100	140	mV/mT
"Zero" component	B_0	$V_Q = 0.5\,V$	–35		35	mT
Linearity error (referred to $V_Q = \frac{V_S}{2}$)				2		%
Temperature coefficient	TC	$T_{amb} = 0–70°C$		0.4		mT/K

Pin configuration and application circuit



Output characteristic without adjustment $V_Q = f(B)$



Magnetically Operated Contactless Switches with Dynamic Outputs

Type	Ordering code
SAS 241	Q67000–S50
SAS 241 S4	Q67000–S50-S4

The ICs SAS 241 and SAS 241 S4 are contactless switches which are operated by a magnetic field. The outputs with open collectors permit wired AND connections for generation of encoded signals. The outputs Q_1 and Q_2 generate signals of identical phase which are independent of the duration of action of the magnetic field. The south pole of the magnetic field must act vertically on the surface marked with the notch.

Maximum ratings

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S		–0.5		20	V
Output current	I_{Q1}, I_{Q2}				30	mA
Thermal resistance	R_{thsamb}				170	K/W
Junction temperature	T_j				150	°C
Storage temperature	T_s		–40		125	°C

Range of operation

Supply voltage						
SAS 241	V_S		4.75		18	V
SAS 241 S4	V_S		4.75		5.25	V
Ambient temperature	T_{amb}		0		70	°C

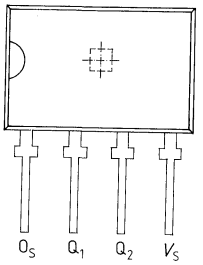
Electrical characteristics at $V_S = 5\,V$, $T_{amb} = 0$ to 70° C, unless otherwise specified

Supply current	I_S	$B < B_{OFF}$	1		3	mA
	I_S	$B > B_{ON}$, Q_1, Q_2 = H			3.5	mA
	I_S	$B > B_{ON}$, Q_1, Q_2 = L	1.5		6	mA
Flux density for "ON"	B_{ON}				0.065	T
Flux density for "OFF"						
SAS 241	B_{OFF}		0.01			T
	B_{OFF}	$V_S = 18\,V$	0.005			T
SAS 241 S4	B_{OFF}		0.005			T
Maximum temperature deviation referred to 25° C	$\Delta B_{ON}/B_{OFF}$		–0.005		0.005	T
Hysteresis	B_{Hy}		0.004	0.01	0.015	T
Output current	I_{Q1}, I_{Q2}	$B \leqq B_{OFF}$			10	µA
Output voltage	V_{Q1}, V_{Q2}	$I_{Q1} = I_{Q2} = 16\,mA$			0.4	V

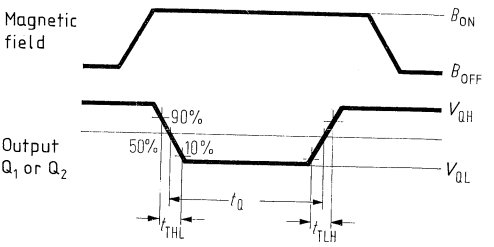
Delay times ($V_S = 5\,V$, $T_{amb} = 25°\,C$)

Transition time	t_{THL}	between 90 and 10 %			1	µs
	t_{TLH}	between 10 and 90 %			2	µs
Output pulse width	t_Q	between 50 and 50 %	15	20	40	µs

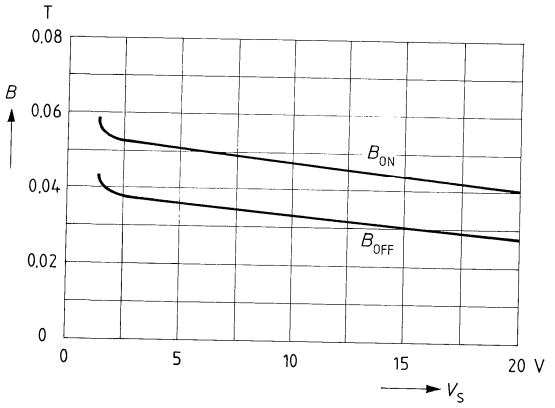
Pin configuration



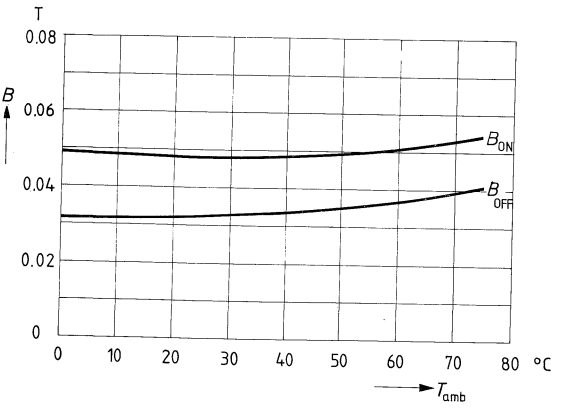
Pulse diagram



$B_{ON}, B_{OFF} = f(V_S)$, typ.



$B_{ON}, B_{OFF} = f(T_{amb})$, typ.



Magnetically Operated Contactless Switches with Static Outputs

SAS 251
SAS 251 S4
SAS 251 S5

Type	Ordering code
SAS 251	Q67000–S47
SAS 251 S4	Q67000–S47-S4
SAS 251 S5	Q67000–S47-S5

The ICs SAS 251, SAS 251 S4, and SAS 251 S5 are contactless switches which are operated by a magnetic field.
The outputs with open collectors permit wired AND connections for generation of encoded signals. The outputs Q_1 and Q_2 generate signals of identical phase. The south pole of the magnetic field must act vertically on the surface marked with the notch.

Maximum ratings

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage						
SAS 251	V_S		–0.5		30	V
SAS 251 S4, SAS 251 S5	V_S		–0.5		20	V
Output current	I_{Q1}, I_{Q2}				30	mA
Thermal resistance	R_{thsamb}				170	K/W
Junction temperature	T_j				150	°C
Storage temperature	T_s		–40		125	°C

Range of operation

Supply voltage						
SAS 251	V_S		4.75		27	V
SAS 251 S4	V_S		4.75		5.25	V
SAS 251 S5	V_S		4.75		18	V
Ambient temperature	T_{amb}		0		70	°C

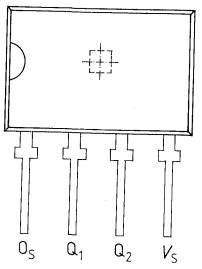
Electrical characteristics at $V_S = 5\,V$, $T_{amb} = 0$ to 70° C, unless otherwise specified

Supply current	I_S	$B < B_{OFF}$	1		3	mA
	I_S	$B > B_{ON}$	1.5		6	mA
Flux density for "ON"	B_{ON}				0.065	T
Flux density for "OFF"						
SAS 251, SAS 251 S5	B_{OFF}		0.01			T
SAS 251	B_{OFF}	$V_S = 27\,V$	0.005			T
SAS 251 S5	B_{OFF}	$V_S = 18\,V$	0.005			T
SAS 251 S4	B_{OFF}		0.005			T
Maximum temperature deviation referred to 25° C	$\Delta B_{ON}/B_{OFF}$		–0.005		0.005	T
Hysteresis	B_{Hy}		0.004	0.01	0.015	T
Output leakage current	I_{Q1}, I_{Q2}	$B < B_{OFF}$			10	µA
Output voltage	V_{Q1}, V_{Q2}	$I_{Q1} = I_{Q2} = 16\,mA$			0.4	V

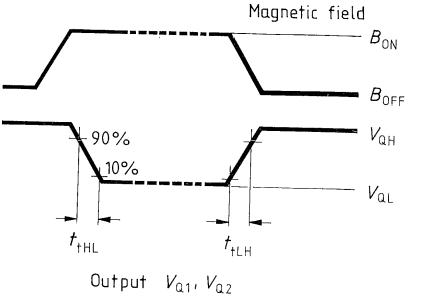
Delay times ($V_S = 5\,V$, $T_{amb} = 25°\,C$)

Transition time	t_{THL}	between 90 and 10%			1	µs
	t_{TLH}	between 10 and 90%			2	µs

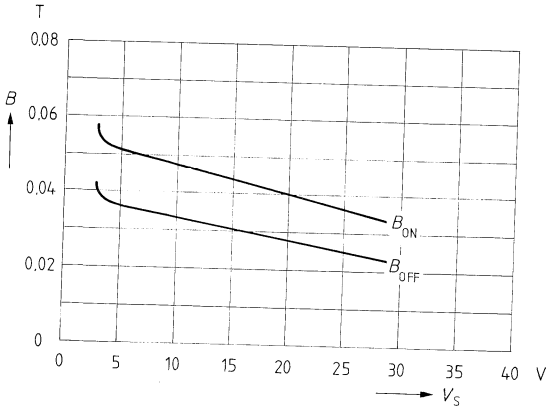
Pin configuration



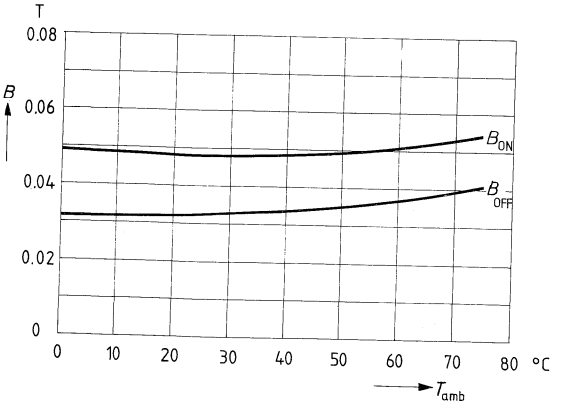
Pulse diagram



B_{ON}, $B_{OFF} = f(V_S)$, typ.



B_{ON}, $B_{OFF} = f(T_{amb})$, typ.



Type	Ordering code
SAS 261	Q67000–S59
SAS 261 S4	Q67000–S59–S4

The ICs SAS 261 and SAS 261 S4 are contactless switches which are operated by a magnetic field. If a sufficiently high flux density is present ($B = B_{ON}$) and an H signal is present at the enable input, the open collector output Q switches from H to L. The south pole of the magnetic field must act vertically on the surface marked with the notch.

Maximum ratings

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S		–0.5		20	V
Output current	I_Q				30	mA
Input voltage at E	V_E		–0.5		5	V
Thermal resistance	R_{thsamb}				170	K/W
Junction temperature	T_j				150	°C
Storage temperature	T_s		–40		125	°C

Range of operation

Supply voltage						
SAS 261	V_S		4.75		18	V
SAS 261 S4	V_S		4.75		5.25	V
Ambient temperature	T_{amb}		0		70	°C

Electrical characteristics at $V_S = 5\,V$, $T_{amb} = 0$ to 70° C, unless otherwise specified

Supply current	I_S	$V_E = 0.4\,V$, B any value			500	µA
	I_S	$V_E = 2.5\,V$, $B > B_{ON}$	1.5	5	5	mA
	I_S	$V_E = 2.4\,V$, $B < B_{OFF}$	1		3	mA
Flux density for „ON"	B_{ON}				0.065	T
Flux density for „OFF"						
SAS 261	B_{OFF}		0.01			T
	B_{OFF}	$V_S = 18\,V$	0.005			T
SAS 261 S4	B_{OFF}		0.005			T
Maximum temperature deviation referred to 25° C	$\Delta B_{ON}/B_{OFF}$		–0.005		0.005	T
			0.004	0.01	0.015	T
Hysteresis	B_{Hy}		2.4			V
H-input voltage at E	V_{IH}				0.8	V
L-input voltage at E	V_{IL}	$V_E = 2.4\,V$			0.5	µA
H-input current at E	I_{IH}	$V_E = 0.8\,V$			5	µA
L-input current at E	I_{IL}	$V_E = 0.8\,V$, B any value			10	µA
Output leakage current	I_{Qlk}	$V_E = 2.4\,V$, $B < B_{OFF}$, $V_Q = V_S$			10	µA
						µA
Output voltage	V_Q	$V_E = 2.4\,V$, $B > B_{ON}$, $I_Q = 16\,mA$			0.4	V

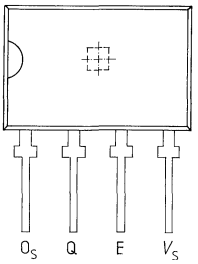
Delay times ($V_S = 5\,V$, $T_{amb} = 25\,°C$)

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Propagation delay E to Q	t_{PHL}	between 50 and 50 %		0.4	3	µs
	t_{PLH}	between 50 and 50 %		1	4	µs
Transition time	t_{THL}	between 90 and 10 %			1	µs
	t_{TLH}	between 10 and 90 %			2	µs

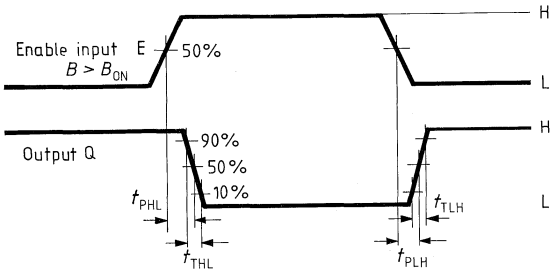
Truth table

Enable input	$B > B_{ON}$	$B < B_{OFF}$	Output Q
L	X		H
L		X	H
H	X		L
H		X	H

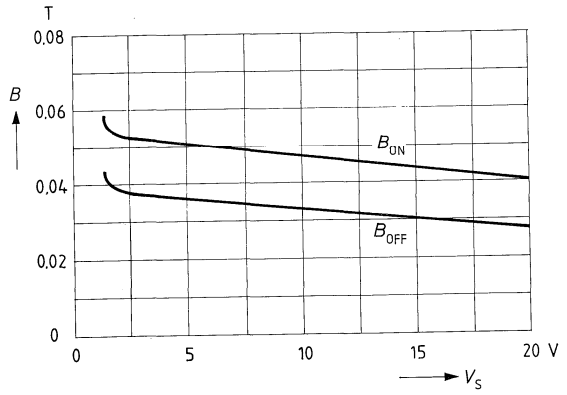
Pin configuration



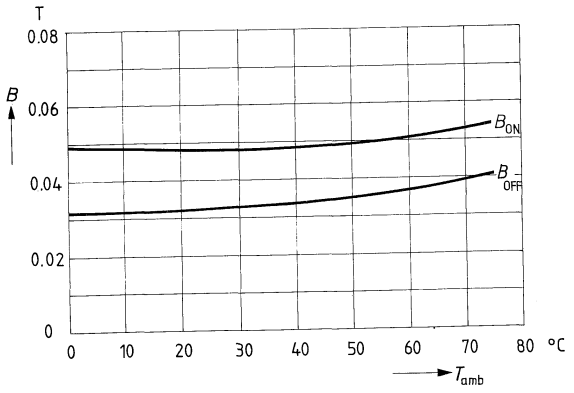
Pulse diagram



$B_{ON}, B_{OFF} = f(V_S)$, typ.

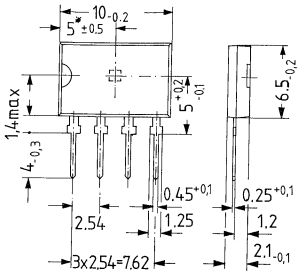


$B_{ON}, B_{OFF} = f(T_{amb})$, typ.



Package Outline Drawings of the Hall Circuits

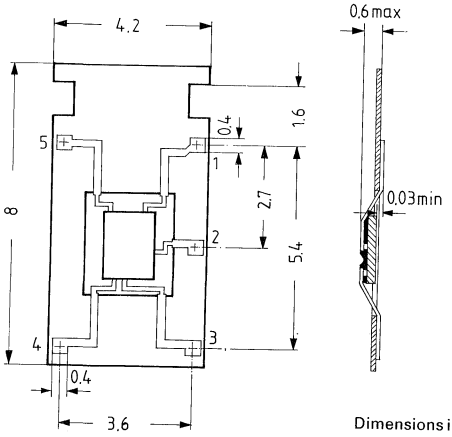
Plastic flat package



Weight approx. 0.5 g
Dimensions in mm

* SAS 221 S2, S4 = 4,7 ±0,5

Micropack



Dimensions in mm

Circuits for Special Functions

Preliminary data

Type	Ordering code
S 89	Q67000-H1694

A frequency divider with the preselectable divider ratios 50/51, 100/101, 100/102, 200/202. Maximum input frequency 500 MHz for divider ratios 100/102 and 200/202 or 250 MHz for divider ratios 50/51 and 100/101. The S 89 is specially suitable for use as a prescaler for the S 187 (see description later in this section).

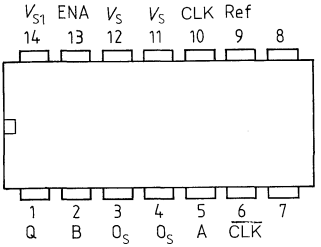
Main application: Prescaler in dual-modulus frequency dividers.

Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage	V_S	−0.3	7	V
Input voltage ENA	V_{ENA}	−0.3	15	V
Input voltage A, B	V_{AB}	−0.3	7	V
Input voltage CLK	V_C	−0.3	$V_S+0.3$	V
Output voltage Q1, output cut off	V_{Q1}	−0.3	12	V
External voltage at Ref.	V_{Ref}	−0.3	$V_S+0.3$	V
Output current at Q_1, output conducting	I_{Q1}		4	mA
Junction temperature	T_j		125	°C
Storage temperature	T_s		125	°C
Thermal resistance				
system-ambient	R_{thsamb}		75	K/W
system-case	$R_{thscase}$		45	K/W

Range of operation

		Test conditions	Lower limit B	Upper limit A	Unit
Supply voltage	V_s		4.5	5.5	V
Maximum input frequency	f_{Cmax}	ratios 50/51, 100/101	250[1])		MHz
Maximum input frequency	f_{Cmax}	ratios 100/102, 200/202	500[1])		MHz
Minimum input frequency, sinusoidal	f_{Cmin}	ratios 50/51, 100/101	20[1])		MHz
Minimum input frequency, sinusoidal	f_{Cmin}	ratios 100/102, 200/202	40[1])		MHz



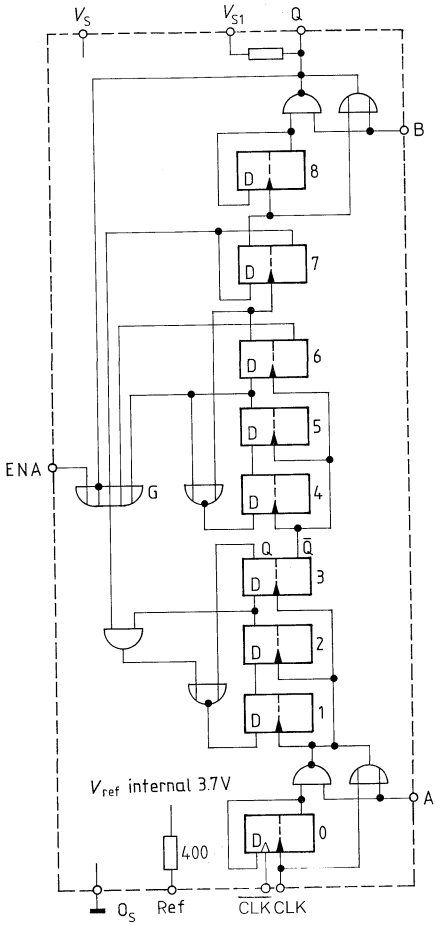
Pin configuration
top view

[1]) Amplitude (peak-to-peak) at CLK: 250 mV ≦ V_{Cpp} ≦ 400 mV, V_S: 4.75 ≦ V_S ≦ 5.5 V.

Electrical characteristics in the operating range
($T_{amb} = -30$ to $80°C$)

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_S		4.75		5.25	V
Supply current	I_S	Input and output open		55	85	mA
L-input voltage at ENA	V_{ENAL}				1	V
H-input voltage at ENA	V_{ENAH}	$T_{amb} = -30°C$	3.2			V
H-input voltage at ENA	V_{ENAH}	$T_{amb} = 25°C$	3			V
H-input voltage at ENA	V_{ENAH}	$T_{amb} = 80°C$	2.8			V
H-input current at ENA	I_{ENAH}	$V_{ENA} = V_{ENAH} = f(T_{amb})$		0.17	0.3	mA
H-input current at ENA	I_{ENAH}	$V_{ENA} = 9V$		1.7	3	mA
L-input voltage at A or B	V_{ABL}				1.5	V
H-input voltage at A or B	V_{ABH}		$V_S-0.1$		$V_S+0.1$	V
H-input current at A or B	I_{ABH}	$V_{AB} = V_S$		0.5	1	mA
Threshold voltage at CLK	V_C	$V_S = 5V$		3.7		V
Static switching voltage deviation at CLK (CLK and Ref connected)	V_{Cpp}		250		1600	mV
Switching voltage deviation at C at 500 MHz (CLK and Ref connected)	V_{Cpp}	$V_S = 5V$	250		400	mV
Output voltage at Q_1	V_{Q1}	$I_{Q1} = 3.2mA$			0.4	V
R between Q_1 and Q_2	R_{Q2}		1.8	2.5	3.2	kΩ

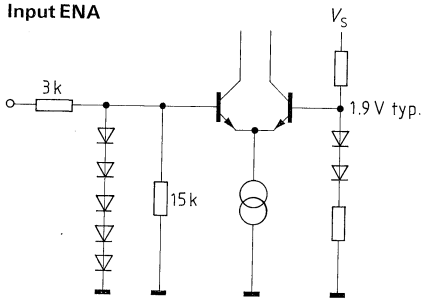
Block diagram



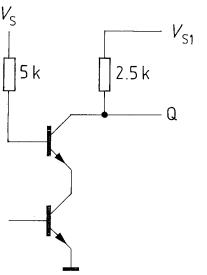
Truth table

A	B	ENA	f_C/f_Q
H	H	H	200
H	H	L	202
H	L	H	100
H	L	L	102
L	H	H	100
L	H	L	101
L	L	H	50
L	L	L	51

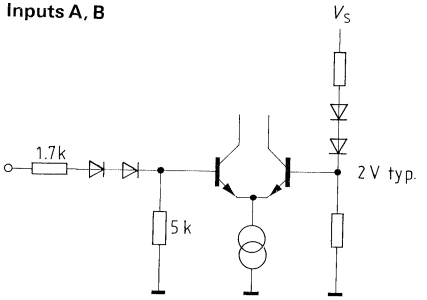
Input ENA



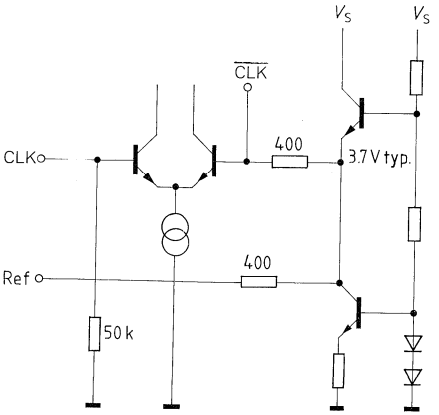
Outputs Q_1 and Q_2



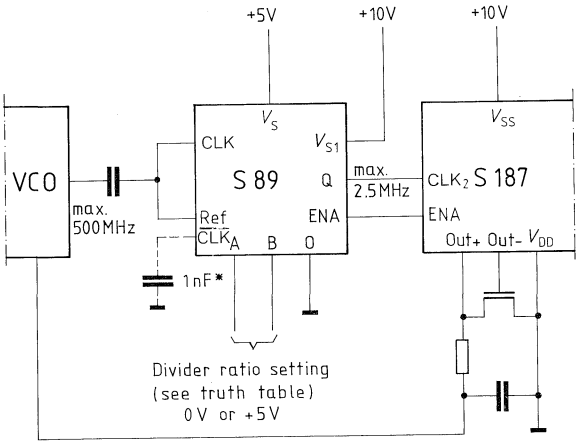
Inputs A, B



Inputs C and Ref



Application example
Prescaler for PLL circuits S 187



*) Capacitor is necessary only for operation close to the limit frequency and the maximum input sensitivity.

Type	Ordering code
S 178	Q67100–Z84

The S 178 is a highly integrated MOS circuit in p-channel metal-gate technology with enhancement and depletion transistors, with the following technical characteristics:

The **video pulse generator** produces the synchronization, control and erase signals required for the control of cameras, mixers and other equipment.

The following signals are generated:

- Strobing signal A
- Synchronization signal S
- Horizontal pulse H
- Vertical pulse V
- Clamping pulse K_t
- Horizontal strobing pulse A (H)
- Double line frequency $H/2$ } → $H/2 + V_R$ signal with external signal mixing
  One half vertical frequency V_R }

Special properties

All pulses are derived digitally from an input frequency, corresponding to a pulse scheme, with a duty cycle of 1:1.

Pulse lengths are in accordance with the old CCIR and EIA standards.

A modified IC in accordance with the new CCIR standard is currently being prepared.

The following 5 pulse schemes have been programmed in a fixed way (through 3-bit coding and line-number coding):

525 lines (60 Hz) required input frequency 1.008 MHz
625 lines (50 Hz) required input frequency 1.000 MHz
735 lines (60 Hz) required input frequency 1.4112 MHz
875 lines (50 Hz) required input frequency 1.400 MHz
1023 lines (60 Hz) required input frequency 1.96416 MHz

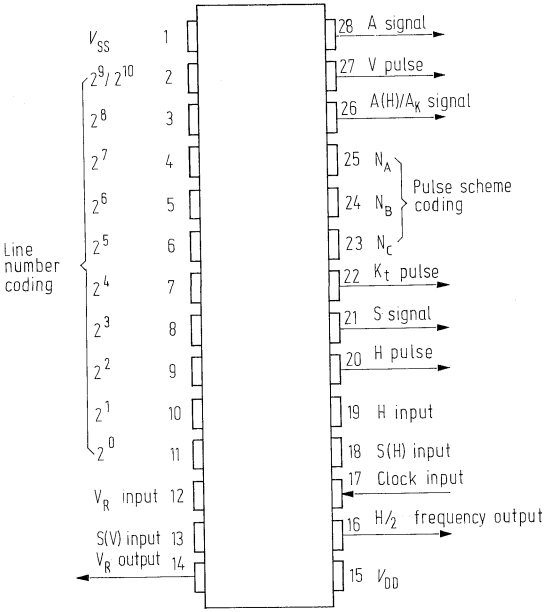
Deviating from the above, any line number between 512 and 1535 lines can be programmed.

It should be noted, however, that a frame frequency of 50 Hz (partial picture duration 20 ms) or 60 Hz (16.66), respectively, is achieved.

The following relation applies:

Input frequency f_I = 64 : line period H
= 32 · line number Z · line frequency f_B

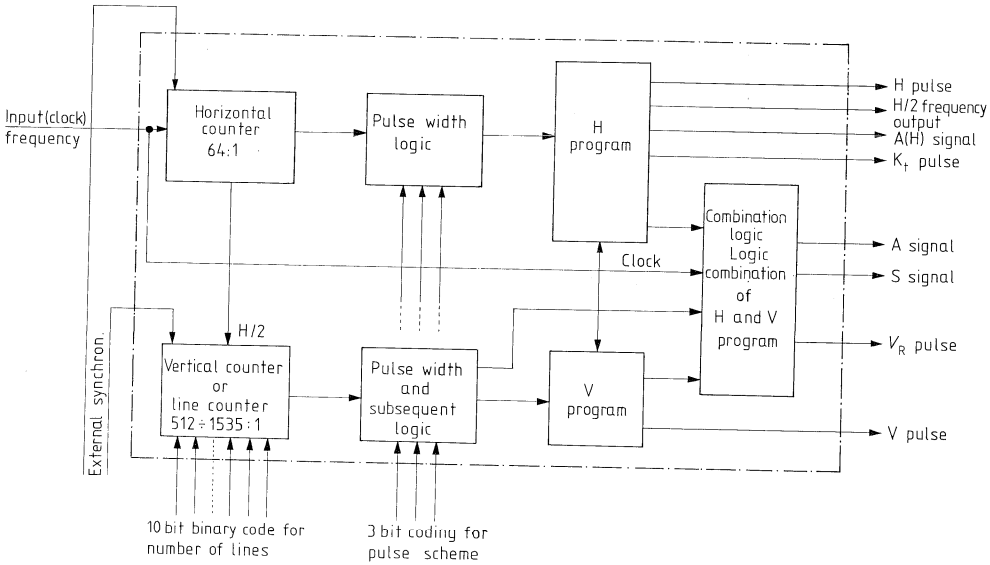
Pin configuration,
top view



Inputs	Pin No.	Outputs	Pin No.
10 inputs for line number coding	2–11	8 outputs for:	
3 inputs for line scheme coding	23–25	A signal	28
		S signal	21
2 inputs for external synchronization		A (H) pulses	26
with $H/_2 + V_R$ signal for pulses at H and V_R	19, 12	K_t pulses	22
2 inputs for external synchronization with		H pulse	20
S signal for pulses from S(H) and S(V)	18, 13	V pulse	27
1 input for the clock frequency	16	$H/_{2\,syn}$ frequency	16
2 inputs for the voltage supply (V_{SS} and V_{DD})	1, 15	V_R pulse	14

With appropriate external components, the $H/_2 + V_R$ signal can be derived from mixing the $H/_{2\,syn}$ frequency and the V_R pulse.

Block diagram



Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage	referred	V_{DD}	−12	0.3	V
voltage at all pins	to $V_{SS} = 0$ V	V	−20	0.3	V
Input current ($V_I = 0.3$ V; $V_{SS} = 0$ V)		I_I		100	μA
Storage temperature		T_s	−55	125	°C
Ambient temperature		T_{amb}	0	75	°C

Electrical characteristics: ($T_{amb} = 25°$ C)

a) Operating voltage: $V_{SS} - V_{DD} = 10$ V ±5%

e.g., if 0 V and −5 V are applied to an external TTL logic, the MOS circuit requires a $V_{SS} = 0$ V and $V_{DD} = -10$ V supply for direct driving.

b) Supply current: typically 40 mA

c) Input levels: direct driving with TTL output levels

$V_{SS} \geqq$ log. H $\geqq V_{SS} - 1.5$ V
$V_{DD} \leqq$ log. L $\leqq V_{SS} - 4.3$ V
fan out ≧ 1 TTL input load

d) Output level: when loaded with 1 TTL-input (log. H → 40 μA; log. L → −1.6 mA)

$V_{SS} \geqq$ log. H $\geqq V_{SS} - 2.6$ V
$V_{DD} \leqq$ log. L $\leqq V_{SS} - 4.6$ V

e) Rise and fall times: in a range defined by d) ≦ 100 ns

f) Maximum input frequency: lower limit ≧ 2 MHz typ. 2.8 MHz

1. Description of function

The main units of the pulse generator are horizontal and vertical counters (see block diagram). The horizontal counter, with a counting ratio 64:1, divides the input frequency down to double the line frequency $H/_2$.

An additional logic ensures that in the moment of turning on, or due to a noise pulse, no undefined condition of the counter flipflops can occur.

The multiples of the input frequency, programmed for all line schemes, are derived from coincidence of the counter; thereby, all pulses are temporarily created one clock period ahead, or pre-synchronized.

Post-synchronization is done with the following clock pulse transition, immediately at the output. Consequently, delays caused by the finite switching speed of the circuit elements are eliminated. Reference transition for all pulses is $H/_2$ syn.

The vertical counter, designed as an 11-bit asynchronous counter, is driven with double the line frequency $H/_2$. All pulses derived from this frequency are a definite integer multiple of $H/_2$ and occur delayed with respect to this frequency, however, before $H/_2$ syn. Thereby the later occurring post-synchronization of $H/_2$ syn is made possible as well.

The vertical counter can be programmed externally for a particular line number. This is done by comparing the externally coded line number with the counter position, in the case of equality internally resetting it and starting anew with the following $H/_2$-transition.

As external programming has been done for the line number of the complete picture, however, the counter is operated with double the line number, the vertical signals will occur per partial picture.

Through the external 3-bit coding, programming is done internally for the chosen pulse scheme, i.e. the corresponding circuit elements for the realization of the H and V program are activated.

The pulses are subsequently either directly connected to the outside or mixed appropriately according to the 3-bit-code in the combination logic and strobed. In any case, a post-synchronization is previously done with the clock transition. Starting of all pulses and the pulse widths are therefore defined in their timing relative to $H/_2$ syn.

2. External synchronization with $H/2 + V_R$ or S-signal

For mixing and superposition of the pictures, the BAS-signals of the individual cameras or Video recorders must be synchronized with respect to each other, i.e. they must agree in line and picture timing. In the case of external synchronization, the external signal must contain these two components: either the horizontal and vertical frequency (for S-signal, S(H) and S(V)) or the (double-)horizontal and one-half vertical frequency (for $H/2 + V_R$).

Of these two H and V components, short pulses are derived at the beginning of the leading edge, and the horizontal and vertical counters are set to a defined position with these pulses. (Approximate values: H-component $\approx$ 300 ns < pulse period
V-component $\approx$ 1 µs < $H/2$)

Due to the timing differences of the leading edges of line frequency H and S (H), being 1.5 periods of the input frequency, in one case the horizontal counter would be set to a wrong position. For this reason inputs have been provided for both horizontal components. They can be used to set the counter, depending on the particular component used, to the appropriate position.

The same is valid for the vertical components of $H/2 + V_R$ and the S signal. The first picture change pulse follows 2.5 or 3 line periods behind the V_R pulse, depending on the scheme. The two inputs provided for the pulses from V_R or S(V), respectively, and the correspondingly coded line scheme enable the proper setting of the vertical counter. Through the possibility of a defined setting of the counters it is ensured that a proper standard pulse scheme is obtained at the outputs even in the case of external synchronization involving different phase conditions of the synchronization signals.

Note:

At the time of setting the horizontal counter to a defined position, the phase relation of the input frequency is undefined and consequently the tolerance of the synchronization would be one clock period (i.e. $\leqq$ 1 µs for 625 lines). By means of an external phase synchronization circuit with frequency multiplication, the input clock can be derived from the vertical component and thereby a defined phase relation of the reset pulse achieved relative to the input clock. Hence a common line deviation (jitter) of < 20 ns absolute value can be achieved.

3. Control

The pulse generator derives the required pulses digitally from the input frequency. As additionally half a clock period is used for the generation of the pulse widths, and as both the leading and trailing edges are used, an input duty cycle of 1:1 is required.

It is therefore recommended to operate the quartz oscillator used at double the input frequency and to divide it 2:1 with an external stage, thereby achieving an accurate duty cycle of 1:1.

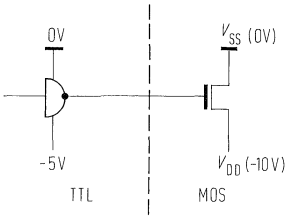
For the line schemes provided the following interrelations hold true:

525 lines	1.008 × 2	→	2.016 MHz
625 lines	1.000 × 2	→	2.000 MHz
735 lines	1.4112 × 2	→	2.8224 MHz
875 lines	1.400 × 2	→	2.800 MHz
1023 lines	1.96416 × 2	→	3.92832 MHz

All inputs of the pulse generator have been designed such that they can directly be controlled by the TTL output level. It must be taken care that the positive supply voltage for the MOS circuit is connected to the positive supply of the TTL logic (for MOS = 10 V, for TTL = 5 V).

Inputs not used must be connected to V_{SS} (log. "H").

Circuit diagram



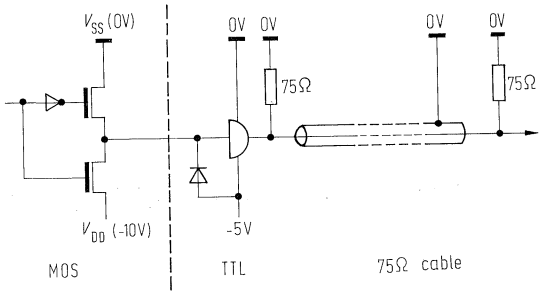
4. Interface to 75 Ω cable

As the outputs of the pulse generator may be loaded with 1 TTL input each as a maximum, a driver stage is required.

Connection according to the circuit diagram shown below.

The additional diode serves as a protection for the TTL-stage against too low an input voltage or against exceeding the permissible power consumption.

As a driver stage for the 75 Ω coaxial cable, the TTL circuit 75 453 (maximum output current 300 mA; pulse delay 11 ns) is recommended.



5. Coding tables

Coding for pulse scheme 1:5

N_A	N_B	N_C		
L	L	L	525 lines	1
L	L	H	625 lines	2
L	H	L	735 lines	3
L	H	H	875 lines	4
H	L	L	1023 lines	5

10-bit dual code for number of lines

1024	512	256	128	64	32	16	8	4	2	1	
2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Connection
L	H	L	L	L	L	L	H	H	L	H	525 lines
L	H	L	L	H	H	H	L	L	L	H	625 lines
L	H	L	H	H	L	H	H	H	H	H	735 lines
L	H	H	L	H	H	L	H	L	H	H	875 lines
L	H	H	H	H	H	H	H	H	H	H	1023 lines

In addition, any other line number may be programmed; however, because of the combination of 2^9 and 2^{10} required to form one input, there is a limitation to 512:1535 lines.

When programming an even line number, the intermediate line is skipped.

e.g.

2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Connection
L	H	L	L	H	H	L	H	H	H	L	624 lines

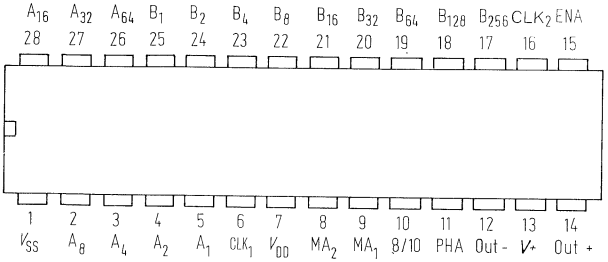
Type	Ordering code
S 187	Q67100–Y199

The S 187 is a highly integrated MOS circuit in p-channel metal-gate technology with enhancement and depletion transistors, featuring the following special technical properties:

- More than 500 000 different frequencies presettable
- 8 different reference frequencies presettable
- High degree of flexibility through appropriate coding
- High reference input frequency
- Integrated phase comparator
- Simple 10 V supply
- Low power consumption even at high frequencies
- Specially suitable programmable diode matrix S 353, (see LSL series) available for frequency selection
- Specially suitable predivider S 89 available for extension up to 500 MHz (see description earlier in this section)

Possible applications

- Multichannel equipment
- Navigation equipment
- Citizen band radio
- Scanning receiver
- Signal generators

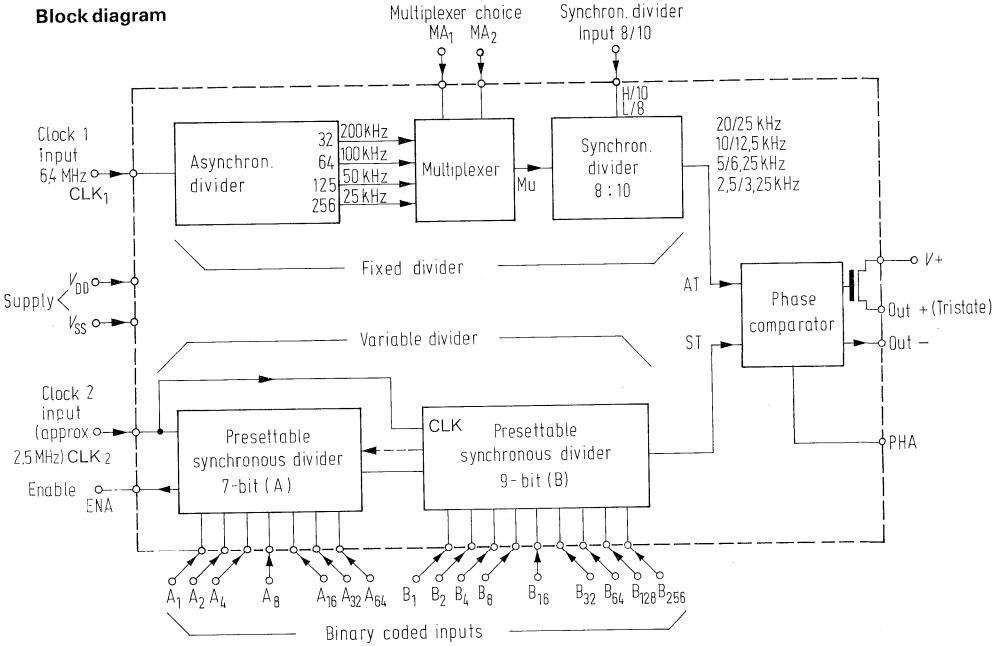


Pin configuration
top view

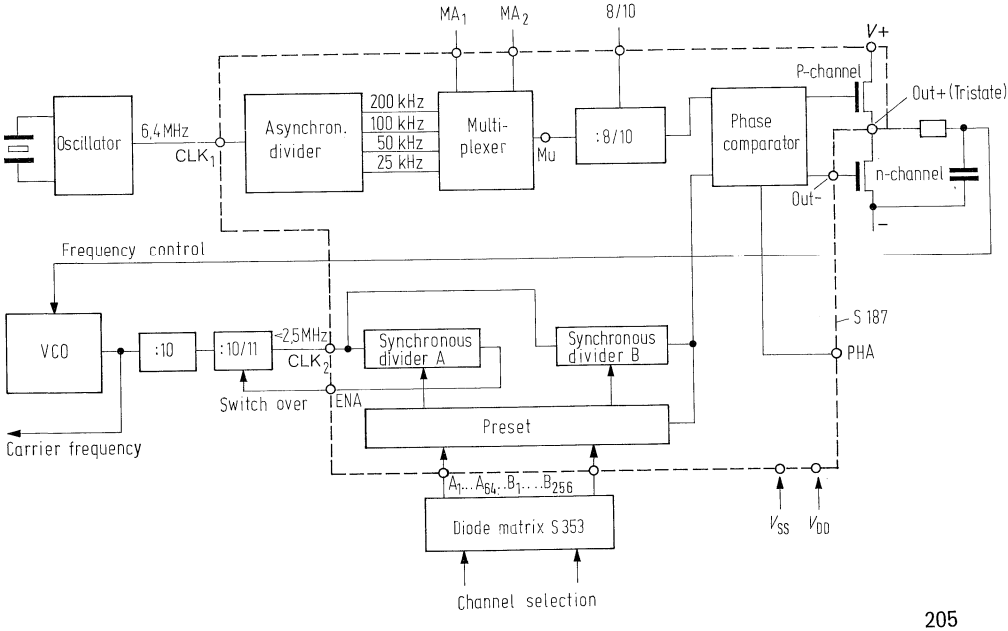
Pin names

Inputs			Outputs		
Abbrev.	Pin		Abbrev.	Pin	
A_1	5	Binary coded inputs for presettable synchronous divider (A) 7 bits	ENA	15	Enable output
A_2	4		PHA		Phase comparator output
A_4	3		out +	14	Output +
A_8	2		out −	12	Output −
A_{16}	28		$V+$	13	Output for the control of external n-channel transistor
A_{32}	27				
A_{64}	26				
B_1	25	Binary coded inputs for presettable synchronous divider (B) 9 bits			
B_2	24				
B_4	23				
B_8	22				
B_{16}	21				
B_{32}	20				
B_{64}	19				
B_{128}	18				
B_{256}	17				
CLK_1	6	Clock input 1 for asynchronous divider (max. 6.4 MHz)			
CLK_2	16	Clock input 2 for synchronous divider (max. 2.5 MHz)			
8/10	10	Divider setting 8 or 10 for asynchronous divider			
MA_1	9	Multiplexer choice 1 and 2			
MA_2	8				
V_{SS}	1	Supply voltages			
V_{DD}	7				

Block diagram



Block diagram of a carrier frequency generator with S 187



Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage } referred to	V_{DD}	15	−0.3	V
Voltage at all pins } $V_{DD} = 0$ V	V	15	−0.3	V
Input current ($V_I = 0.3$ V; $V_{DD} = 0$ V)	I_I		1	mA
Storage temperature	T_s	−55	125	°C
Ambient operating temperature	T_{amb}	−20	70	°C

Electrical characteristics ($T_{amb} = 25°C$)

		Test conditions	Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}	Used as common and reference voltage	0	0	V
Supply voltage $V_{SS\,typ} = 10$ V	V_{SS}	$V_{DD} = 0$ V	9	11	V
Supply current	I_{SS}	$I_{SS\,typ} = 8$ mA		35	mA
Inputs A_1 through A_{64} B_1 through B_{256}, 8/10					
L-resistance	R_{IL}	$C_{in} = 10$ pF to V_{SS}	0	3	kΩ
H-resistance	R_{IH}	Current input "L" max. = approx. 500 µA (short circuit to V_{DD} at $V_{SS} = 10$ V)	100	∞	KΩ
Input CLK_1					
L-input voltage	V_{IL}	$F_{CLK1max} = 6.5$ MHz,	V_{DD}	$V_{SS}-8$	V
H-input voltage	V_{IH}	$t_a = t_f = 25$ ns, $C_{in} = 15$ pF to V_{SS}, pulse width 50 ns min.	$V_{SS}-0.5$	V_{SS}	V
Input CLK_2					
L-input voltage	V_{IL}	$F_{CLK2max} = 2.5$ MHz,	V_{DD}	$V_{SS}-8$	V
H-input voltage	V_{IH}	$t_a = t_f = 50$ ns, $C_{in} = 25$ pF to V_{SS}, pulse width 150 ns min.	$V_{SS}-0.5$	V_{SS}	V

Electrical characteristics ($T_{amb} = 25°C$)

		Test conditions	Lower limit B	Upper limit A	Unit
Inputs MA_1, MA_2					
L-input voltage	V_{IL}	$C_{in} = 10\,pF$	V_{DD}	$V_{SS}-8$	V
H-input voltage	V_{IH}	to V_{SS}	$V_{SS}-0.5$	V_{SS}	V
Outputs OUT+, OUT−	V_{QL}	$I_L = 1\,mA$, $V_{SS} = 10\,V$	9		V
L-output voltage	V_{QH}	$I_H = -1\,mA$, $V_{SS} = 10\,V$		4	V
H-output voltage	I_{VCmax}	1 µA at $T_{amb} = 70°C$			
Output PHA					
L-output voltage	V_{QL}	$I_L = 100\,\mu A$, $V_{SS} = 10\,V$		6.5	V
H-output voltage	V_{QH}	$I_H = -1\,mA$, $V_{SS} = 10\,V$	6.5		V
Output ENA					
L-output voltage	V_{QL}	open-drain			
H-output voltage	V_{QH}	$I_H = 3.5\,mA$, ECL-interface	5		V

Basic functions

The frequency synthesizer S 187 is used for channel selection in the carrier frequency generator. The carrier frequency is generated by a voltage-controlled oscillator (VCO) and after a **preset division** (depending on channel) compared with a crystal-stabilized reference frequency. The output voltage of the frequency comparator controls the VCO.

By appropriate choice of the division, the carrier frequency can be set to a particular multiple of the reference frequency.

Construction and function

Refer to block diagram of a carrier frequency generator including the portion integrated in the S 187.

The following functions are comprised:

a) 8-stage asynchronous divider, input frequency 6.4 MHz max., output frequency selectable 200, 100, 50, 25 kHz.

b) switchable :8/:10-divider,

a) and b) together supply the crystal-stabilized reference frequency (8 possibilities).

c) fully programmable synchronous divider consisting of two interconnected parts; input frequency $\leqq 2.5$ MHz;

1. 7-stage divider A, presettable from :1 through :127-division. After completion of the process this divider is stopped. It is reset and triggered by divider B. Consequently it generates the switching signal for a :10/:11 predivider, which causes a nonius-kind of division; for this purpose the comparator frequency may be adjusted to a higher value. The switching signal (output ENA) must therefore be synchronized with the input clock (delay <300 nsec.).

2. 9-stage divider B, presettable from :2 to :512-division. At the end of the process this divider resets itself and divider A. It supplies the divided carrier frequency for the phase comparator.

d) The phase comparator (see figure) performs the frequency comparison. It possesses 3 possible output combinations (see truth table 1) between which it switches, initiated by $0 \rightarrow 1$ transitions at the inputs (see truth table 2).

In the case of the input frequencies being different, the leading signal switches the output on its side (AT out +, ST out −) to "1"; it remains at this level until the other signal switches it back to "zero".

If both frequencies are equal but different in phase, an output pulse with the width of the phase difference is generated at the leading side with each clock pulse. In the case of both $0 \rightarrow 1$ transitions at the inputs lying within the dwell period, the phase comparator will remain in the "0"-state.

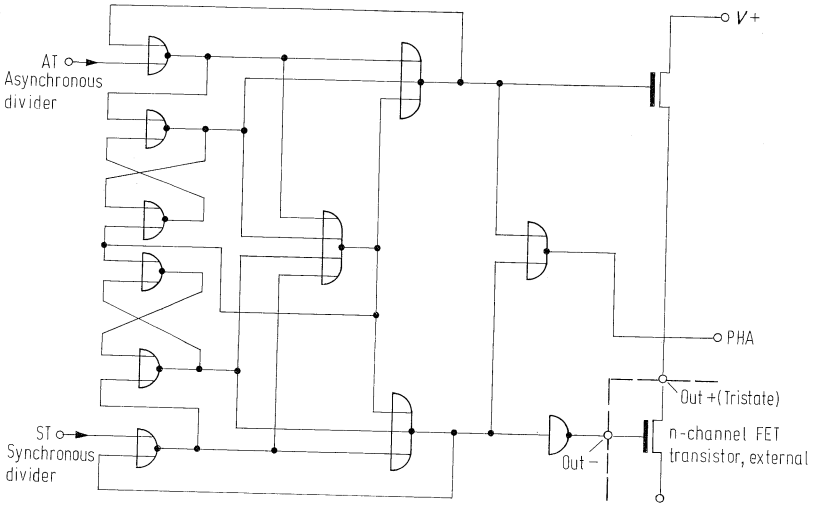
The phase comparator drives a complementary tristate gate, whereby the internal p-channel transistor is driven by the positive output and the external n-channel transistor from the inverted negative output. Consequently, the integration capacitor is charged during an H-level, discharged during an L-level. During a 0-level its output is connected to a high resistance. Therefore the capacitor voltage, and consequently the frequency of the VCO, changes until the $0 \rightarrow 1$-transitions are within one dwell period of the phase comparator at both inputs.

3. Active p-function of the programming inputs. The assignment of individual frequencies to particular speech-channels can externally be done, e.g. by using a 10×16 PROM (diode matrix) which connects the selected programming inputs low-resistively to a negative potential (L), and which loads the non-selected ones only with leakage currents (H).

The equivalent worst case values are: 5 kΩ to V_{DD} (L) or 100 kΩ to V_{DD} (H).

The programming inputs have therefore been provided with an active p-circuit (see figure), which in the H-condition creates an input voltage of $> V_{SS} - 1$ V and in the L-condition an input voltage of $< V_{DD} + 1$ V. This way various ways of driving the inputs are made possible.

Phase comparator



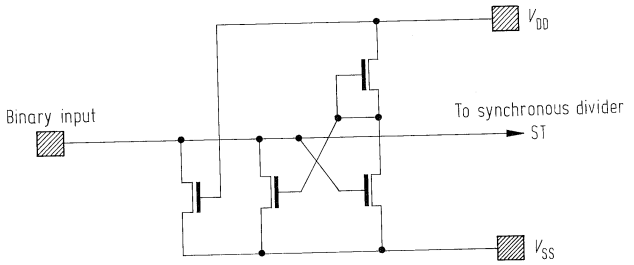
Truth table 1 **Phase comparator**

Condition PHA Phase comparator	Output +	Output –
H	1	0
L	0	1
0	0	0

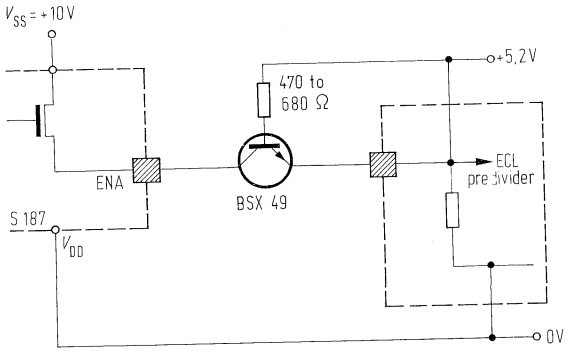
Truth table 2 **Phase comparator**

Output condition PHA Phase comparator	0 → 1-transition at	
	AT Asynchronous divider	ST Synchronous divider
H	H	0
0	H	L
L	0	L

Active p-connection of the programming inputs



Driving an unsaturated ECL predivider stage



Truth tables of dividing ratios for synchronous divider (ST) and asynchronous divider (AT)

a) Inputs 8/10:

H	division by 10
L	division by 8

b) Inputs A_1 through A_{64}:

LSB $= A_1$
MSB $= A_{64}$

Condition H LLL LLL corresponds to division by 1

c) Inputs B_1 through B_{256}:

LSB $= B_1$
MSB $= B_{256}$

Condition H LLL LLL LL corresponds to division by 1

d) Inputs MA_1 and MA_2:

MA_1	MA_2	Frequency setting at MU
L	L	25 kHz
H	L	50 kHz
L	H	100 kHz
H	H	200 kHz

Digital Multimeter Circuit

Type	Ordering code
S 190	Q67100–Z96

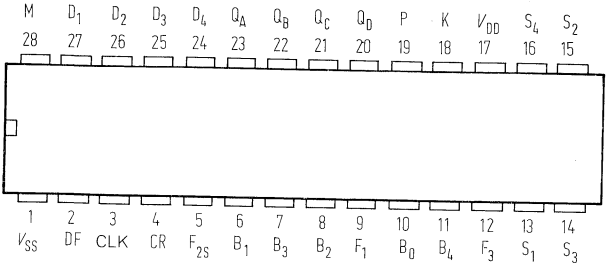
The S 190 is a highly integrated MOS circuit in p-channel metal gate technology, with enhancement and depletion transistors.

It features the following special technical properties:

- 3¾-digit decade display (±5999 max.)
- Automatic polarity indication
- Automatic range selection
- Range extension
- Overflow indication (blinking)
- 4-decade counter
- Multiplex BCD-outputs
- Multiplex oscillator
- Counting clock oscillator
- Measuring phases for dual slope method

Particular properties

- Low power consumption
- C-MOS compatible
- Fully static

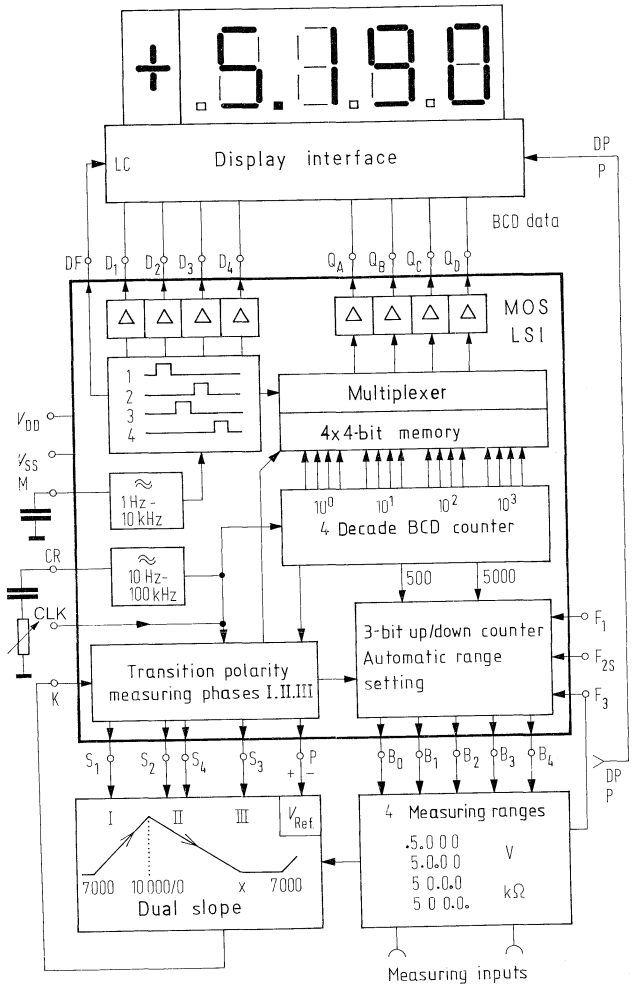


Pin configuration
top view

Pin names

Inputs			Outputs		
Abbrev.	Pin		Abbrev.	Pin	
K	18	Analog input	S_1	13	Measuring phase outputs for dual slope
			S_2	15	
			S_3	14	
CR	4	Oscillator-clock connection input for counters and control signals	S_4	16	
CLK	3	External oscillator clock input for counters and control signals	B_0	10	Measuring range outputs
			B_1	6	
			B_2	8	
			B_3	7	
			B_4	11	
M	28	Oscillator-clock connection input for multiplexer	P	19	Polarity indication output
			D_1	27	Position selection outputs
			D_2	26	
			D_3	25	
			D_4	24	
F_1	9	Measuring range extension inputs			
F_{2S}	5				
F_3	12				
			Q_A	23	BCD-outputs
			Q_B	22	
			Q_C	21	
			C_D	20	
V_{DD}	17	Supply voltage			
V_{SS}	1				
			DF	2	Frequency output for LCD

Block diagram



Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage } referred to	V_{DD}	−20	0.3	V
Voltage at all pins } $V_{SS} = 0\,V$	V	−20	0.3	V
Input current ($V_I = 0.3\,V$; $V_{SS} = 0\,V$)	I_I		1	mA
Storage temperature	T_s	−55	125	°C
Ambient temperature	T_{amb}	−20	70	°C

Electrical characteristics: ($T_{amb} = 25°\,C$, unless otherwise stated)

		Test conditions	Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}	Used as common and reference voltage	0	0	V
Supply voltage $V_{SS\,typ.} = 12\,V$	V_{SS}	$V_{DD} = 0\,V$	8	14	V
All inputs except K:		$V_{DD} = 0\,V$			
L-input voltage	V_{IL}	(at C_L, $F_{typ.} = 30\,kHz$,	0	$V_{SS}-7$	V
H-input voltage	V_{IH}	duty cycle 1:1)	$V_{SS}-0.5$	V_{SS}	V
K-input:					
L-input voltage	V_{IL}		0	$V_{SS}-7$	V
H-input voltage	V_{IH}		$V_{SS}-2$	V_{SS}	V
Outputs D_1, D_2, D_3, D_4, Q_A, Q_B, Q_C, Q_D, P:					
L-output voltage	V_{QL}	$I_L = 25\,\mu A$	0	1	V
H-output voltage	V_{QH}	$I_L = -200\,\mu A$	$V_{SS}-1$	V_{SS}	V

		Test conditions	Lower limit B	Upper limit A	Unit
Outputs B_0, B_1, B_2, B_3, B_4, S_1, S_2, S_3, S_4:					
L-output voltage	V_{QL}	$I_L = 50\,\mu A$	0	1	V
H-output voltage	V_{QH}	$I_L = -200\,\mu A$	$V_{SS}-1$	V_{SS}	V
Output DF:					
L-output voltage	V_{QL}	$I_L = 50\,\mu A$	0	1	V
H-output voltage	V_{QH}	$I_L = -50\,\mu A$ $F_{typ.} = 50$ Hz, for LCD	$V_{SS}-1$	V_{SS}	V
Power consumption	P	$V_{DD} - V_{SS} = -12$ V without power dissipation at the outputs		60	mW
Timing conditions:					
Delay time	t_d	between S_3 and K (load = 200 pF, 10 MΩ) measured at 50 % of the H-value		4	µs

Oscillator specifications

Counting and control oscillator:

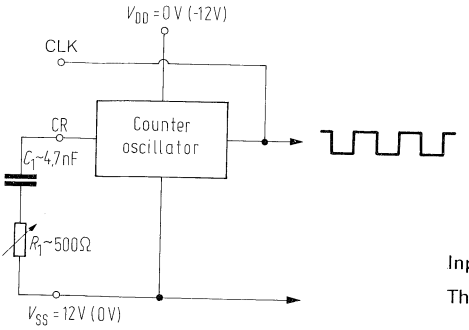
External components: R, C
Number of pins: 2 (CR, CLK)
Frequency parameters:

Parameters	Lower limit A	Typ.	Upper limit B	Unit	Remarks
Frequency f		30	100	kHz	
Frequency stability $F(V) = \frac{\Delta f}{f_G} \cdot 100$		±3		$\frac{\%}{V}$	$\Delta f = f(V_{SS} = 12\,V) - f_G$ [2]), $T_{amb} = 25°C$, $V_{SS} = 12\,V \pm 1\,V$
Frequency stability $F(T) = \frac{\Delta f}{f_G} \cdot 100$		±0.8[1])	±1	$\frac{\%}{°C}$	$\Delta f = f(T = 25°C) - f_G$, $T_{amb} = 0°$ to $70°C$, $V_{SS} = 12\,V$

[1]) Calculated value
[2]) $f_G = f$ at $V_{SS} = +12\,V$ and $T_{amb} = 25°C$

Modes of operation:

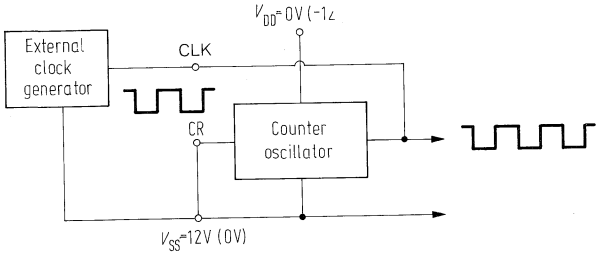
Circuit 1



Input CLK open

The oscillator drives the decade counter

Circuit 2

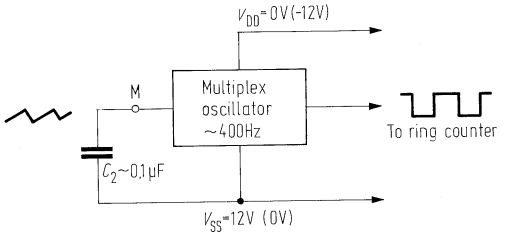


Input CR connected to V_{SS}
Input CLK: External clock
The oscillator becomes ineffective and the decade counter is driven externally.

Multiplex oscillator:

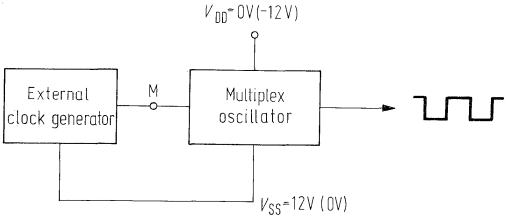
External connection:	R, C
Number of pins:	1 (M)
Frequency parameter:	$f_{typ.}$ = 400 Hz

Circuit 1



Multiplex oscillator

Circuit 2



Only for testing purposes and $R_i \approx 0$
Clock generator is loaded by M

Functional description S 190

General

The circuit comprises the logic functions for a digital multimeter, on the basis of the dual-slope-method, with automatic range switching.

By means of four measuring-range outputs, small units with 3¾ digits (compare block diagram on page 215) and four measuring ranges can be realized without additional external components for the range selection. By switching the range logic, up to eight different measuring ranges can be switched automatically; however, decoding of these ranges must be done externally.

Due to the low power consumption of the S 190 (60 mW), use of a liquid-crystal display permits the design of small units operated economically by batteries.

The maximum display is 6000. 6000 steps mean a relatively small analog circuit requirement, however, they permit the measuring of voltages between 100 µV and 600 V in the four measuring ranges. When the highest measuring range is exceeded, the value 6000 is displayed. Through an additional blinking circuit, which does not require an additional connection pin, the user is made aware of the measuring range being exceeded.

Function

The block diagram shows a simple unit with four automatically selected measuring ranges. The external analog portion consists of only the analog amplifiers, reference voltage source, and the analog switches for the measuring phase and range switching.
The sequence control and generation of the value measured is done by the S 190. The main portion of the circuit is made up of a four decade BCD-counter which is driven by a counting oscillator contained on the chip, together with an externally connected RC-circuit (according to page 218). (By connecting a clock generator, according to page 219, the counting oscillator may be replaced). At particular periods of timing the contents of the counter is transferred into the 4 × 4-bit memory by means of a strobe pulse derived from the K-input.
The information contained in the memory is transferred by means of a multiplexer in a bit-parallel mode to outputs Q_A through Q_D, whereby outputs D_1 through D_4 indicate the just transferred decimal place (Q_A ≙ LSB, Q_D ≙ MSB; D_1 ≙ units digit, D_4 ≙ thousands digit, active condition = high level). To ensure reliable driving of the memories in the display interface, e.g. liquid crystal display, the correct BCD-information is maintained at the Q-outputs until after the end of the active condition of the D-outputs. The indication of decimal position occurs in the sequence 1-3-2-4, to avoid flickering when the display units are driven directly.
For the generation of scan-frequency for the multiplexer a second oscillator has been provided on the S 190 (external connection page 219).
Replacement by an external clock generator is possible (compare page 220) but should be used only for testing purposes. The display frequency DF of about 50 Hz required by liquid crystal displays is also derived from the multiplex oscillator.

Measuring sequence

The measuring sequence is also controlled by the BCD-counter, via measuring-phase outputs S_1 through S_4 (compare timing diagram and principle circuit diagram on page 223).

Phase I, integration of measuring voltage

The measuring cycle starts at counter position 7000; at this point output S_1 becomes high, whereby the input voltage is switched to the integrator until counter position 0000 has been reached.
At the moment when the counter jumps from 9.9999 to 0000, the signal level of the comparator (input K) is stored. At this moment phase II is started.

Phase II, integration of reference voltage

Depending on the condition of the comparator, only S_2 or S_4 is activated whereby the reference voltage is switched to the integrator which has a polarity opposite to the previously applied input voltage. With this reference voltage the integrator is reduced until the sensitivity threshold of the comparator has been reached and the signal condition at input K changes. This change of signal activates S_3. The number of counting pulses between counter position 0000 and X is proportional to the measuring voltage. Through the low → high transition of S_3 the counter contents is loaded into the display memory; at this point of time phase III is started.

Measuring sequence

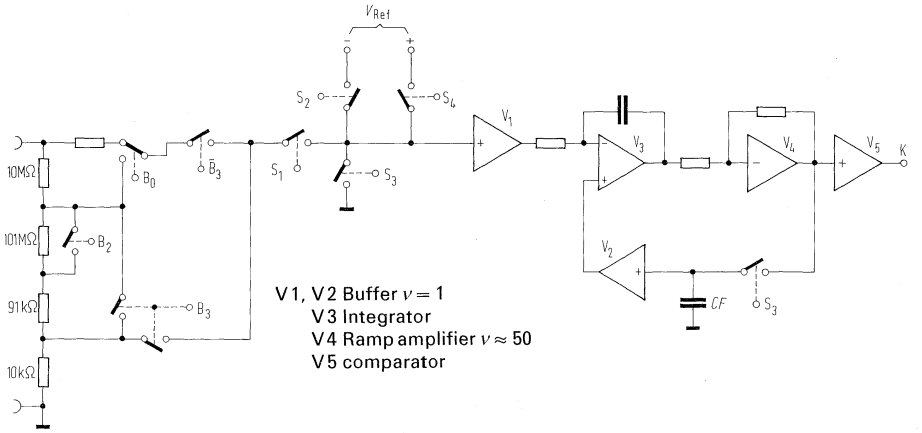
Phase III, zero regulation

In this process the input of the AD-converter is set to zero and the resulting error voltage is stored in capacitor C_F. An error voltage is compensated by a feedback loop. The duration of phase I is determined by the counter frequency and the fixed number of 3000 counting steps. For a 30 kHz counting frequency, phase I lasts exactly 100 ms. The longer the integration time, the better the suppression of noise voltages superimposed on the measuring signal. If the duration of the noise voltage period is contained in the integration time as an even number, this noise is suppressed completely. As noise voltages can be expected to occur especially at line frequency, 100 ms integration time constitute a favourable compromise between integration time and noise voltage suppression. The duration of phase II is determined by the level of the measuring voltage. If the measuring voltage is too large, the integrator cannot be discharged during the 6000 counting steps available as a maximum; consequently, at step 6000 phase III is initiated. Hence, the integrator will have assumed the correct starting position at the beginning of phase I which follows.
For excessive measuring voltages the display is therefore 6000. In order to bring the incorrectness of this display to the user's attention, the pseudo-decade HHHH is made active at the outputs, synchronously to signal S_1; thereby a blinking effect of approx. 3 Hz is obtained.

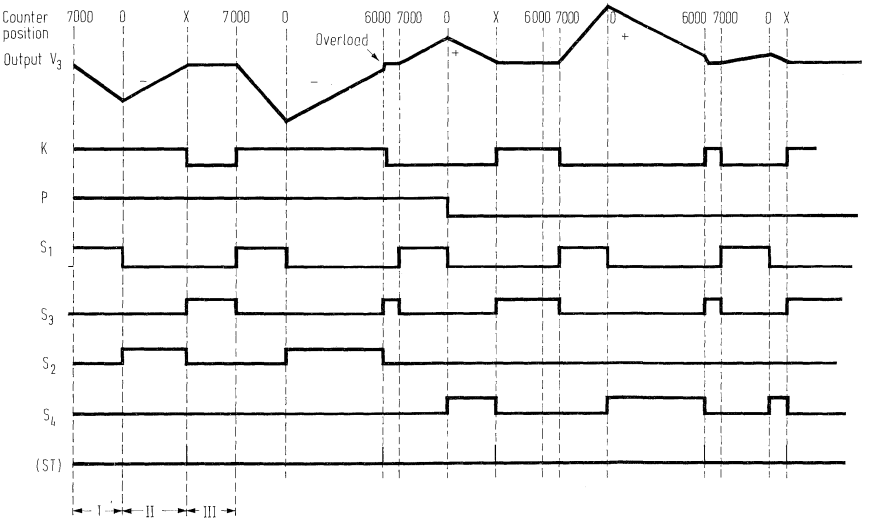
Automatic range switching

The measuring range is changed whenever the measuring result has been $\geqq 5500$ or < 500. For $n \geqq 5500$ the range counter (3 bit up/down counter) is stepped up by one count, for $n < 500$ stepped down by one, whereby the counter is blocked on the lowest or highest digit position, respectively. The range selection can be controlled through control inputs F_1, F_{2S} and F_3.
When the control inputs F_1, F_{2S} and F_3 are in a low condition, the counter can move within the lower 5 positions up or down. Should it be in a higher position, it can step only downward until the "free zone" has been reached; the decoder produces correct values also for counter positions outside the "free zone", so that the system adjusts itself.
By an H-signal at input F_1 the correlation between the counter position and decoder output can be changed. Thereby it is made possible to perform range setting for the voltage and resistance ranges and the control of the decimal point in a simple unit with four measuring ranges without external decoding. Input F_3 is used to set the counter to the highest level. The highest measuring range is activated and maintained as long as F_3 is kept at a high level. For example, thereby the range 500.0 V is activated, which is an advantage for quick overview-measurements.
A high level at input F_{2S} has the effect that the outputs of the range counter are directly transferred to the outputs; 8 different ranges are then available which must be decoded by external means. In the case of $F_{2S} = H$, the "free zone" of the counter is expanded to the full counting range; the prevention of "running wild" is maintained.

Schematic of the analog divider (example for a simple unit)



Pulse diagram
AD converter



Phase { I Integration of measuring value
II Integration of reference voltage
III Zero regulation

Automatic range selection
Truth table

No.	Q_3	Q_2	Q_1	F_1	F_{2S}	F_3	B_0	B_1	B_2	B_3	B_4
0	L	L	L	L	L	L	H				
1	L	L	H	L	L	L		H			
2	L	H	L	L	L	L			H		
3	L	H	H	L	L	L				H	
4	H	L	L	L	L	L				H	H
5	H	L	H	L	L	L				H	H
6	H	H	L	L	L	L				H	H
7	H	H	H	L	L	L				H	H
10	L	L	L	H	L	L		H			
11	L	L	H	H	L	L		H			
12	L	H	L	H	L	L			H		
13	L	H	H	H	L	L				H	
14	H	L	L	H	L	L					H
15	H	L	H	H	L	L					H
16	H	H	L	H	L	L					H
17	H	H	H	H	L	L					H
2 X	Q_3	Q_2	Q_1	X	H	L	X	Q_1	X	Q_2	Q_3
30	H	H	H	L	L	H				H	H
31	H	H	H	H	L	H					H
32	H	H	H	X	H	H	X	H	X	H	H

Q_1, Q_2, Q_3 internal outputs of the up/down counter

The truth table for setting the measuring ranges should be understood as follows:

The range outputs $B_0 \ldots B_4$ are intended to directly drive the five possible decimal places of a 4-decade display. Simple units with 4 measuring ranges have been taken into consideration. For example, in the case of voltages the measuring ranges with F_1 = low are:

B_0	.5000 V
B_1	5.000 V
B_2	50.00 V
B_3	500.0 V

The total measuring range therefore comprises 0.1 mV through 599.9 V.
For resistance measuring, however, F_1 must be high:

B_1	5.000 kΩ
B_2	50.00 kΩ
B_3	500.0 kΩ
B_4	5000. kΩ

The total measuring therefore comprises 1 Ω through 5.999 MΩ.
Hence, using control input F_1, a choice of one of the two groups is basically possible.

The range outputs are also intended to directly drive the appropriate four selection relays without additional logic gating. When the automatic range selection (e.g. after turn-on) has not yet found the correct range, some measuring range is expected to be shown anyway. This side-condition is considered in the truth table of vectors 0 . . . 17.

It should be noted, however, that Q_1, Q_2, and Q_3 in the truth table are internal outputs of the internal up/down counter. It is also possible to select one of 5 measuring ranges automatically. To do this the 4th and the 5th measuring ranges are separated by external gating at F_1 = low (whereby $MB_4 = B_3; \overline{B}_4$ and $MB_5 = B_4$). MB_4 is measuring range 4, MB_5 is measuring range 5.

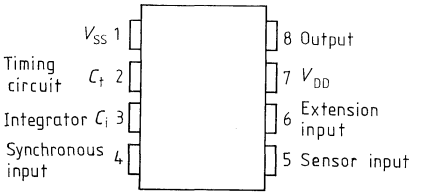
F_{2S} = high causes an extension to all eight possible measuring ranges. The range selected appears at outputs B_1 (= Q_1), B_3 (= Q_2), and B_4 (= Q_3) dual-coded. Hence, vectors 20-27 of the truth table are fixed.

Type	Ordering code
S 566 A	Q67100–Z135
S 566 B	Q67100–Z120

The ICs S 566, implemented in PMOS depletion technology, permit construction of a digital electronic dimmer. The output is switched on and off and the required brightness is set via a single sensor or via an equivalent extension input.

Special features

- Sensor operation – no mechanically operated switch components
- Operation is possible from several points (extensions) by means of sensors or push buttons
- Can be interchanged with electromechanical wall switches in conventional light installations
- High interference immunity
- The set brightness value remains stored during short mains voltage interruptions with a duration $\leqq 1$ s
- Low power dissipation
- Only a small number of peripheral components required



Pin configuration
top view

Maximum ratings
(without external protective circuitry)

		Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}	–20	0.3	V
Input voltage at pins 1, 2, 3, and 8	V_I	–20	0.3	V
Input voltage at pins 4, 5, and 6	V_I	–20		V
Input current at pins 4, 5, and 6	I_I		800	µA
Ambient temperature	T_{amb}	0	80	°C
Storage temperature	T_s	–55	125	°C

Electrical characteristics (T_{amb} = 0 to 80° C, all voltage ratings referred to V_{SS} = 0 V)

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_{DD}		–13	–15	–18	V
Supply current	I_{DD}	V_{DD} = –15 V, T_{amb} = 25° C		1.0	1.4	mA
Supply current if synchronization signal is missing	I_{DD}	V_{DD} = –15 V, T_{amb} = 25° C		0.4	0.5	mA
Input reverse current	I_I	V_I = V_{SS} –10 V, T_{amb} = 25° C			3	µA
Input capacitance	C_I	V_I = 0 V, f = 1 MHz			5	pF
Sensor input						
H-input voltage	V_{IH}	With series resistor 10 MΩ, operating from 220 V mains supply	V_{SS}–2			V
L-input voltage	V_{IL}		V_{DD}		V_{SS}–8	V
Positive H-input current	I_{IH}				35	µA
Trigger transition (H-L transition)	t_{THL}			220 V mains sine wave		
Frequency with active signal	f	Synchronized with 50/60 Hz clock at synchronization input		50/60		Hz
Extension input						
H-input voltage	V_{IH}		V_{SS}–2			V
L-input voltage	V_{IL}		V_{DD}		V_{SS}–8	V
Positive H-input current	I_{IH}				35	µA

Electrical characteristics (T_{amb} = 0 to 80° C, all voltages referred to V_{SS} = 0 V)

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Synchronization input						
H-input voltage	V_{IH}	With series resistor	$V_{SS}-2$			V
L-input voltage	V_{IL}	1.5 MΩ, operating from	V_{DD}		$V_{SS}-8$	V
Positive H-input current	I_{IH}	220 V mains supply			240	µA
Trigger transition (H-L transition)	t_{THL}		220 V mains sine wave			
Frequency	f			50/60		Hz
Output						
H-output voltage	V_{QH}	$V_{DD}=-15$ V, $I_Q=2$ mA	$V_{SS}-6$		V_{SS}	V
L-output voltage	V_{QL}	$V_{DD}=-15$ V,	V_{DD}		$V_{DD}+0.3$	V
H-L transition time	t_{HLQ}				20	µs
L-H transition time	t_{LHQ}				20	µs
H-pulse width	t_{QH}			40		µs

Operation of the inputs

Potential during the positive half-cycle of the mains phase.

Function	Sensor input	Extension input
Operated	L	H
Not operated	H	L

The potential during the negative half cycle has no effect.

Functional description

The S 566 is controlled by means of a single sensor. The duration of contact with the sensor is used as a criterion for distinguishing the instructions. Input signals which are shorter than approximately 60 ms are not evaluated. This immunity time is used to suppress unwanted signals.

Switching on and off

Short touch (60–400 ms) of the sensor area switches the lamp on or off, depending on its preceding state.

Setting of the brightness (dimming)

If the sensor is touched for a longer period (> 400 ms), the conduction angle is continuously varied. It runs across its control loop of 30 to 150° (e.g. bright-dark-bright) in approximately 7 s and continues this sequence until the finger is removed from the sensor.

Control behavior

The two variants S 566 A and S 566 B differ in their control behavior.

S 566 A: When the circuit is switched on, maximum brightness is always set. Dimming is controlled starting from the minimum brightness. If dimming is restarted control continues in the same direction (e.g. "brighter").

S 566 B: When the circuit is switched off, the currently selected brightness is stored and used again when the circuit is switched on again. Dimming always starts at this stored value, its direction being reversed for subsequent dimming operations

Extensions

The switching and control functions can also be performed from extensions, which are connected to an extension input provided specifically for this purpose. The central unit and the extensions are equivalent. Electronic sensor switches or mechanical push buttons may be connected to the extensions.

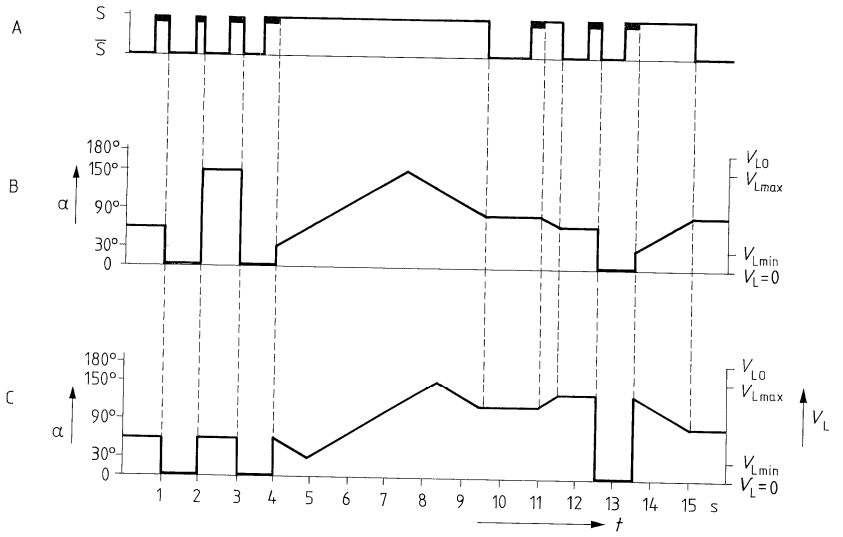
Behavior in the case of mains failure

With the recommended external circuitry, the current state is maintained for at least 1 s in the case of a mains failure. If the mains supply is interrupted for longer periods, the circuit returns to the off state. Across the extension lines, running in parallel to a neutral conductor or ground line, a large 50 Hz interference voltage may arise. After a mains failure simulation of an input signal can thus be caused in the circuit. In order to avoid this, it is recommended that a compensating capacitance C_c with a maximum value of 470 nF (sufficient for a line length of approximately 90 m) be connected.

General

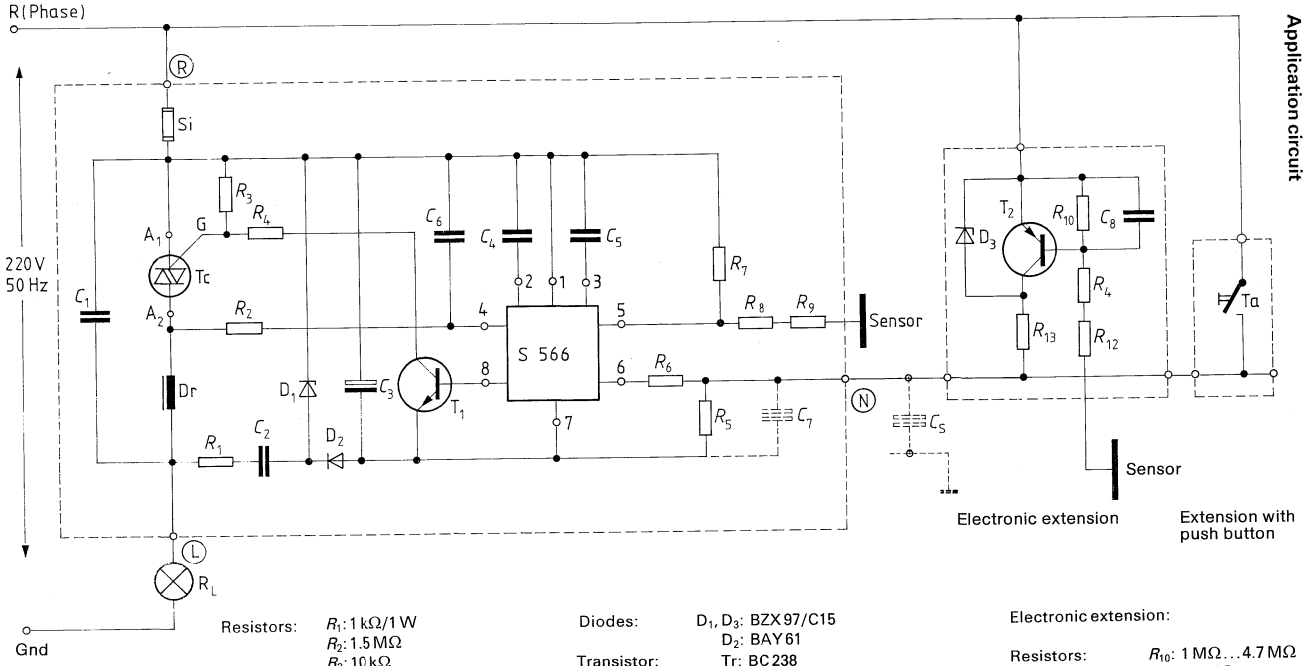
All time specifications shown below are referred to a mains frequency of 50 Hz. For a mains frequency of 60 Hz, the times ar shortened accordingly.

Control behavior



Control behavior of the S 566: Conduction angle α versus the control signal
A: Control signal S = Sensor touched (■ < 0.4 s, – > 0.4 s)
S̄ = Sensor not touched
B: S 566 A
C: S 566 B

Application circuit



Resistors: R_1: 1 kΩ/1 W
R_2: 1.5 MΩ
R_3: 10 kΩ
R_4: 120 Ω
R_5: 220 kΩ
R_6: 470 kΩ
R_7: 0.5 MΩ–4.7 MΩ
R_8, R_9: 4.7 MΩ

Capacitors: C_1: 0.15 µF/220 V ~
C_2: 0.2 µF/220 V ~

Electrolytic capacitor C_3: 47 µF
C_4, C_5: 47 nF
C_6: 470 pF/220 V ~
C_7: Compensating capacitance
C_S: Leakage capacitance to ground

Diodes: D_1, D_3: BZX 97/C15
D_2: BAY 61

Transistor: Tr: BC 238

Triac and choke dependent on the switching power. Triac series recommended: TXC 10, TXD 10

e.g.: 300 W: TXC 10 K 60
600 W: TXC 10 K 60 M

At 110 V/60 Hz mains supply:
C_2 = 0.68 µF/160 V
C_5 = 100 nF

Electronic extension:

Resistors: R_{10}: 1 MΩ...4.7 MΩ
R_{11}, R_{12}: 4.7 MΩ
R_{13}: 27 kΩ/2 W

Capacitor: C_8: 1 nF

Diode: D_4: BZX 97/C 15

Transistor: T_2: BC 308

The suggested application circuit handles the following functions:

- Mains supply for the circuit (R_1, C_2, D_1, D_2, C_3)
- Generation of a suitable synchronization signal for the internal time base (PLL circuit) of the IC (R_2, C_6)
- Amplification of the output signal for driving the triac (T_1, R_3, R_4)
- Protection of the user (R_8, R_9 and R_{11}, R_{12})
- Sensitivity adjustment of the sensor (R_7, R_{10})
- Protection of the circuit against incorrect polarization (R_5, R_6, R_{13}, D_4)
  The resistors R_5 and R_6 can be omitted if no extension is connected.
  In this case, pins 7 and 6 should be interconnected.
- C_4, C_5 are necessary for internal functions.

Type	Ordering code
SAJ 141	Q67100–N62

The SAJ 141 is an asynchronous counter in MOS depletion technology. At three open-drain outputs, it generates the dividing ratios 1000:1, 100:1, or 10:1 of the input frequency. Counted are the LH-transitions.

The IC contains a second input with a higher switching threshold for applications in which high noise immunity is required.

A special reset arrangement provides that the first LH-transition appears at the corresponding output not before 10, 100 or 1000 inputs have occurred.

Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}	–20	0.3	V
Input voltage	V_I	–20	0.3	V
Output current	I_Q	–15	0	mA
Ambient temperature (range 1)	T_{amb}	–0	70	°C
Storage temperature	T_s	–55	125	°C

Static characteristics ($T_{amb} = 25°C$)

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_{DD}		−16		−4.75	V
Supply current	I_{DD}		−5	−3		mA
H-input voltage	V_{IH1}	also for reset input	−1.2		0.3	V
L-input voltage	V_{IL1}	also for reset input	−16		−4.5	V
H-input voltage	V_{IH2}		−2.5		0.3	V
L-input voltage	V_{IL2}		−16		−8	V
H-output voltage	V_{QH}	$R_Q = 10\,k\Omega$	−2			V
L-output voltage	V_{QL}	$R_Q = 10\,k\Omega$			$V_{DD}+0.3$	V
H-input resistance	R_{IH}		10			MΩ
L-input resistance	R_{IL}		10			MΩ
Permissible output current	I_Q		−10			mA

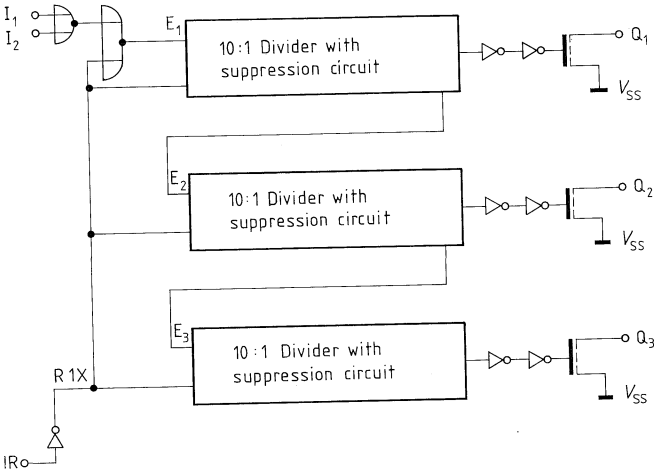
Dynamic characteristics

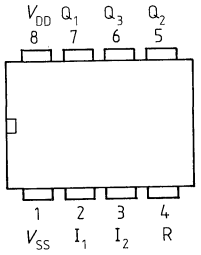
Input frequency	f_i		0		1	MHz
Pulse width	t_{WLI}		450		∞	ns
Pulse dwell	t_{WHI}		450		∞	ns
HL-transition	t_{THLI}				0.3	ms
LH-transition	t_{TLHI}				0.3	ms

at $f =$ MHz, division 10:1

Pulse width	t_{WHQ}		2			µs
Delay time	t_{DLH}	$C_Q = 10\,pF$		0.8	2	µs
HL-transition time	t_{THLQ}	$R_Q = 10\,k\Omega$			3	µs
LH-transition time	t_{TLHQ}	$R_Q = 10\,k\Omega$		0.4	1	µs

Block diagram

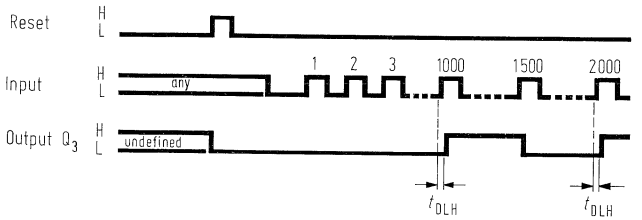


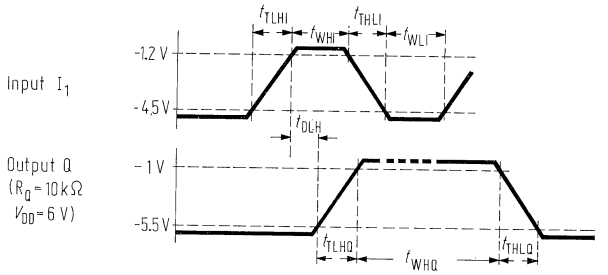


Pin configuration
top view

I = Inputs
Q = Outputs
R = Reset input

Timing diagrams

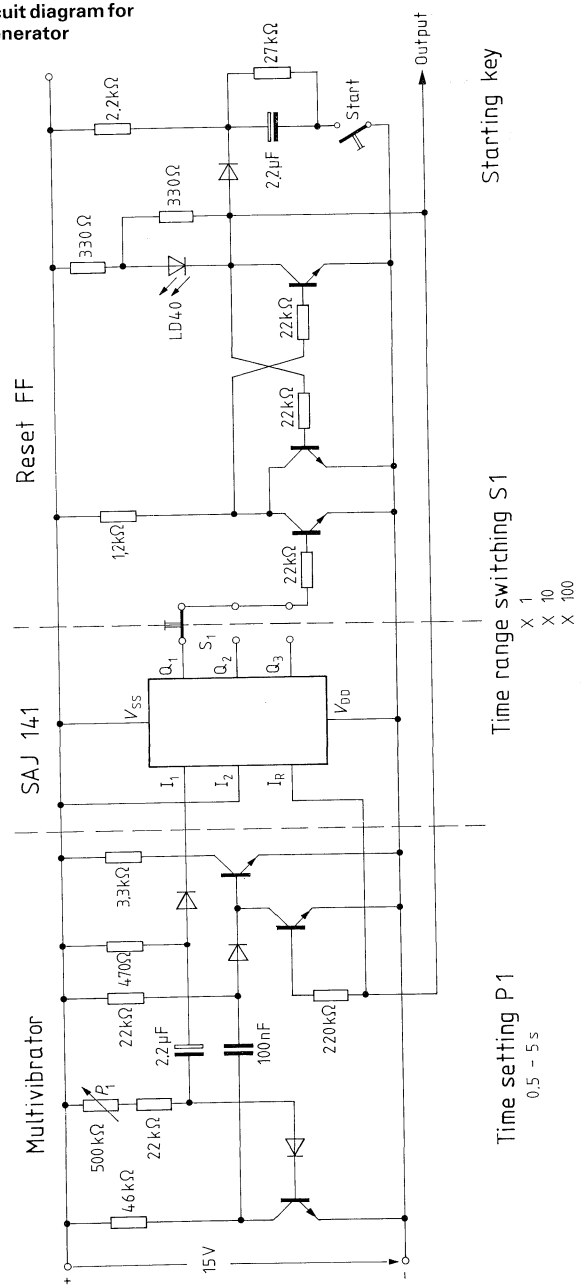




Inputs I_1 and I_2 are gated with each other

Input	Level	Function
I_1	L	I_2 blocked
I_1	H	LH-transitions at I_2 are counted
I_2	L	I_1 blocked
I_2	H	LH-transitions at I_1 are counted

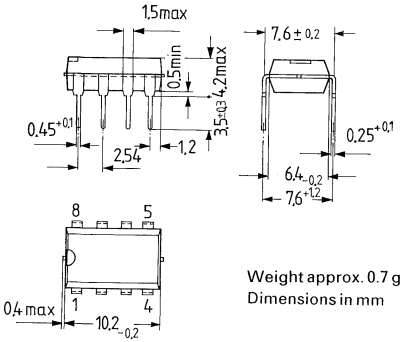
Example of a circuit diagram for a timing pulse generator



All transistors BC 107 or similar, all diodes BA 127 or similar

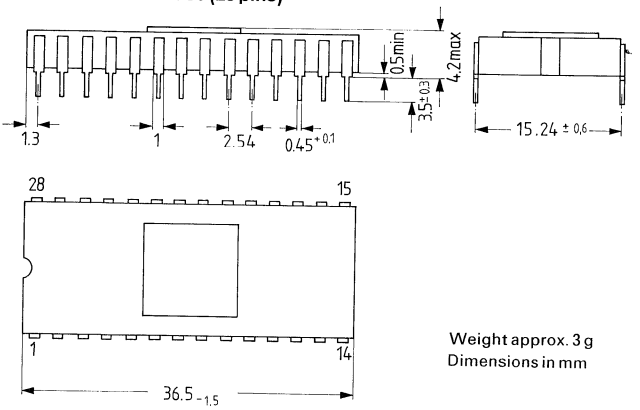
Package Outline Drawings for Special Function Circuits

Plastic plug-in package 20 A 8 DIN 41 866 (8 pins DIP)



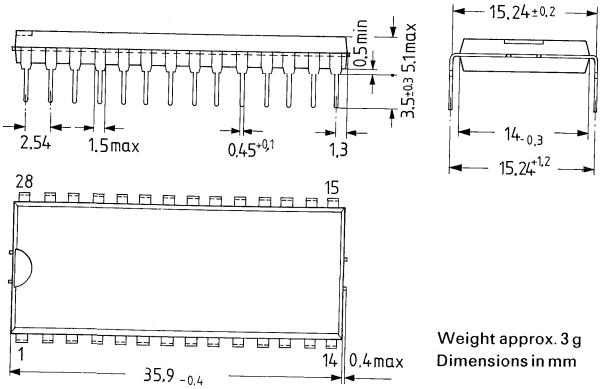
Weight approx. 0.7 g
Dimensions in mm

Metal-ceramic case (28 pins)



Weight approx. 3 g
Dimensions in mm

Plastic plug-in package 20 A 28 DIN 42 866 (28 pins DIP)



Weight approx. 3 g
Dimensions in mm

Circuits for Communications Applications

Type	Ordering code	Package outline
S 120 A 3	Q67100–Z4	Figure No. 3

The S 120 A 3 is a highly integrated MOS circuit in p-channel high voltage technology with the following properties:

- Dial-pulse generator for indirect number selection
- Clock generation integrated
- Inputs BCD coded
- Single operation or combination with S 121 B possible

Brief description

In connection with the S 121 B, the circuit is suited for indirect number selection. At its input the circuit is BCD coded. It has the functions of clock generation and dial-pulse generation. With appropriate external connections, single application is possible.
I_{stop} (pin 24) on L-level: Normal operation (output of all digits with preset interval until memory is empty).
When I_{stop} is set to an H-level during the *n*th digit: Pulse sequence for *n*th digit is produced completely, further pulse output blocked.
When later I_{stop} assumes an L-level: Generation of the remaining digits until memory is empty; this process will not start before a delay of 0 . . . 1600 ms.

Operation at clock frequency f_C

Maximum permissible clock frequency $f_{Cmax.} = 50\,kHz\,(t' = 20\,\mu s)$

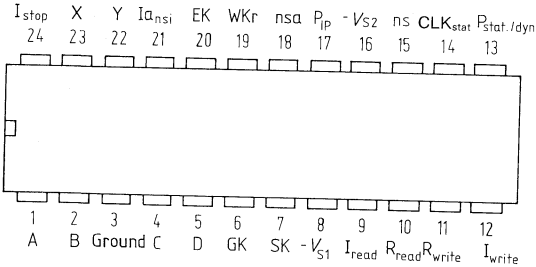
Minimum permissible clock frequency $f_{Cmin.} = 10\,kHz\,(t' = 100\,\mu s)$

The corresponding times $\tau'1 \ldots \tau'5$, $\tau'8$, $\tau'9$ and $t'0 \ldots t'8$ may be calculated according to the following formulae:

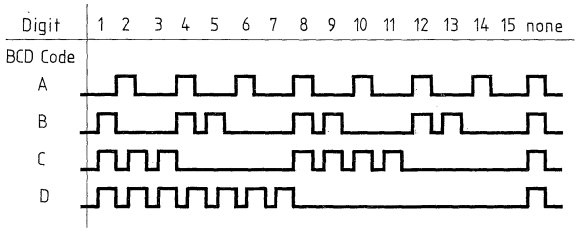
$$\tau' n = \frac{f_o}{f_C}\,\tau n \text{ and } t' n = \frac{f_o}{f_C}\,tn$$

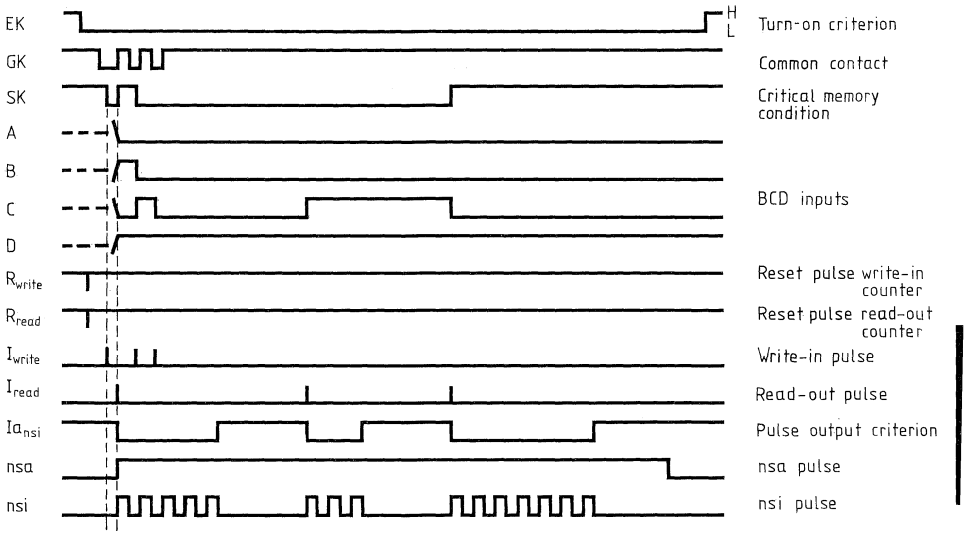
The open inputs are connected to an H- or L-level.

Pin configuration
top view

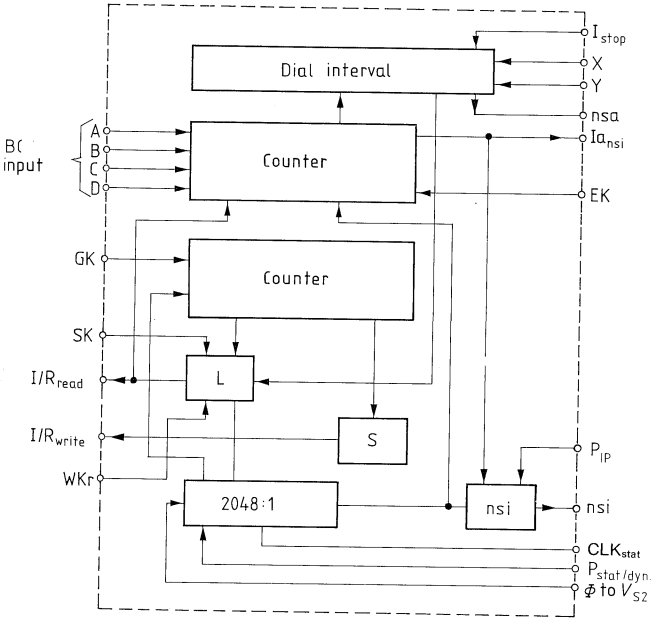


Timing diagram





Block diagram



Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage	$V_{S1} = V_{S2}$	−30	0.3	V
Input voltage	V_I	V_{S1}	0.3	V
Output current	$-I_Q$		10	mA
Ambient temperature	T_{amb}	−25	85	°C
Storage temperature	T_s	−55	125	°C
Power dissipation	P_{tot}		400	mW
Load capacitance	C_0		50	pF

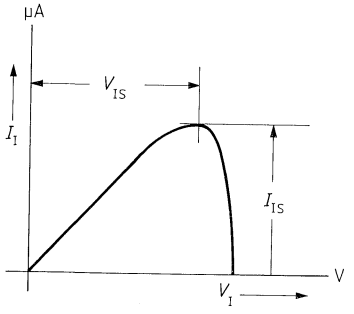
Electrical characteristics

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Ambient operating temperature range	T_{amb}				70	°C
Supply voltage		$V_{S1} = V_{S2}$, quasistatic, $f_0 = 20.48$ kHz, $t_p = 1\,\mu s$	−27		−23	V
	V_{S1}		−27		−23	V
	V_{S2}		−27		−23	V

Static characteristics (all voltages referred to $V = 0$ V)

Power dissipation		$V_{S1} = V_{S2} = -25$ V			165	mW
		$V_{S1} = V_{S2} = -27$ V, outputs unloaded		100	190	mW
		$V_{S1} = -27$ V, $V_{S2} = -27$ V, clocked, $t_p = 1\,\mu s$, $f_0 = 20.48$ kHz		7	10	mW
		$V_{S1} = -27$ V, $V_{S2} = -27$ V, clocked, duty cycle 1:1, $f_0 = 20.48$ kHz			95	mW
Supply current	I_{S1}	$V_{S1} = V_{S2} = -25$ V			6	mA
	I_{S2}				1	mA
Inputs with Schmitt-trigger Input I_{stop} and EK (pin No. 24 and 20)	V_{IH}		−2			V
	I_{IH}	$V_{IH} = -2$ V			150	µA
	V_{IL}		−27		10	V
	I_{IL}	$V_{IL} = -27$ V			10	µA
Input threshold	V_{IS}	$I_{Imax} = 250\,\mu A$	−8	−4	−3	V

Input current $I_I = f(V_I)$



Static characteristics

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Input without Schmitt-trigger	V_{IH}		–2			V
	I_{IH}	$V_{IH} = -2$ V			10	µA
	V_{IL}		–27		–10	V
	I_{IL}	$V_{IL} = -27$ V			10	µA
Outputs	V_{QL}	$I_{QL} = 0$ µA			10	V
		$I_{QL} = 100$ µA			9	V
	V_{QH}	$I_{QH} = 100$ µA	–1			V
Outputs T_{stat}		quasistatic operation				
	V_{QL}	$I_{QL} = 0$	V_{S1}		10	V
	V_{QL}	$I_{QL} = 25$ µA	V_{S1}		9	V
	V_{QH}	$I_{QH} = 25$ µA	–1			V

Dynamic characteristics

		Lower limit B	Typ.	Upper limit A	Unit
Quasistatic operation with S 121 A or B					
Voltage V_{S2}, $f_0 = 20.48$ kHz ($t_0 = 49$ µs)					
Clock amplitude		–23	–25	–27	V
Clock pulse width	t_P	1			µs
Clock rise–fall	t_V			400	µs
Pulse widths					
GK	t_1	20			ms
R_{write}	t_2		6.25		ms
R_{read}	t_3		6.25		ms
I_{write}	t_4		3.12		ms
I_{read}	t_5	3.12		6.25	ms
Dial pulse					
Pulse/pause 1:1	t_6		50		ms
10:6	t_6		62.5		ms
Dial pause					
Pulse/pause 1:1	t_7		50		ms
10:6	t_7		37.5		ms
Dial interval (X = L, Y = L)	t_8		412.5		ms
(X = L, Y = H)	t_8		612.5		ms
(X = H, Y = L)	t_8		812.5		ms
(X = H, Y = H)	t_8		1512.5		ms
Pulse intervals					
GK–GK	τ_9	3			ms
EK–GK	τ_1				
GK–R_{write}	τ_2	3.12		6.25	ms
GK–R_{read}	τ_3	3.12		6.25	ms
R_{write}–I_{write}	τ_4		3.12		ms
I_{write}–I_{read}	τ_5	6.25		25	ms
I_{write}–nsa, $t_p = 1$ µs	τ_6		25	500	µs
I_{read}–nsi (1 st pulse)	τ_7			500	µs
I_{ansi}–nsa (last transition)					
(X = L, Y = L)	τ_8		400		ms
(X = L, Y = H)	τ_8		600		ms
(X = H, Y = L)	τ_8		800		ms
(X = H, Y = H)	τ_8		1500		ms

Dynamic characteristics

Quasistatic, special operation 1

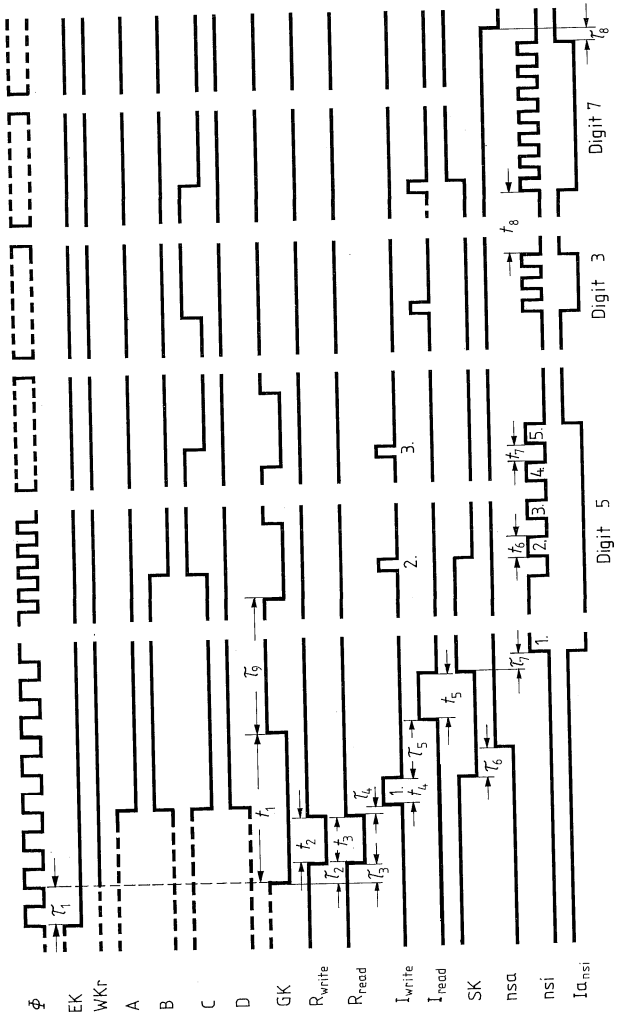
$f_0 = 20.18\,\text{kHz}$, $t_p = \frac{1}{2 \cdot f_0}$

		Lower limit B	Typ.	Upper limit A	Unit
Pulse widths					
EK	t'_1	150			µs
I_{read}	t'_2		6.25		ms
Pulse intervals[1])					
EK–WKr	τ'_1	20			µs
WKr–EK	τ'_2	0			µs
EK–WKr	τ'_3	20			µs
WKr–I_{read}	τ'_4	25 µs		32.5	ms

[1]) only if clock is low at the same time

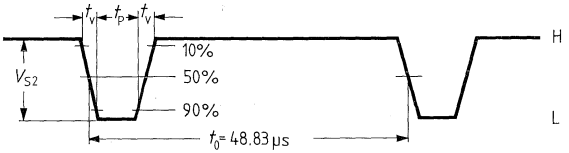
Timing diagram
Operation with S 121 A or B

V_{S2} ($\triangleq \Phi$) clocked, $f_0 = 20.48\,\text{kHz}$, $t_p = \dfrac{1}{2 \cdot f_0}$

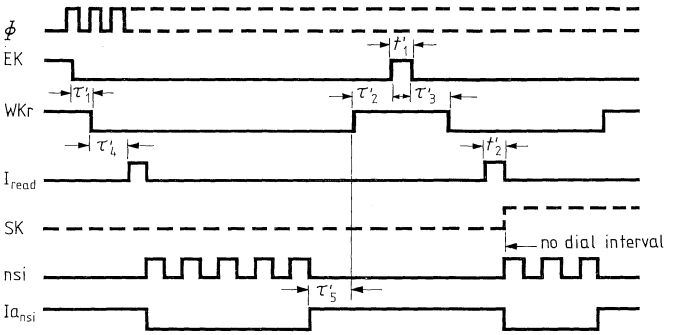


Pulse diagram

Clock voltage $V_{S2}(\hat{=}\Phi)$, $f_0 = 20.48$ kHz



For a special operation, $f_0 = 20.48$ kHz, $t_p = \frac{1}{2 \cdot f_0}$



Type	Ordering code	Package outline
S 121 B	Q67100–Y161	Figure No. 3

The S 121 B is a highly integrated MOS circuit in p-channel high voltage technology with the following properties:

- 16 × 4-bit memory for indirect push button dialling
- BCD-coded inputs
- Integrated write and read counter with comparator
- Memory contents is kept
- Combination with S 120 A 3 or single use

Brief description

The circuit can be used for indirect dialling together with the circuit S 120 A 3.
Circuit S 121 B is used for BCD code. Type S 121 A has an MFV coding at its input. The circuit consists of a 16 × 4-bit memory, the addressing logic and a read-write-counter-comparator. With appropriate connections, single application of the circuit is possible.

The data inputs may be floating. All other inputs are to be connected to an H or L-level. The memory has 16 storage locations of 4 bits each. Resetting the write or read counter leads to memory location 1.

When using the criterion SK (e.g. in connection with the S 120 A 3), 15 digits will be written in, as the 16th writing pulse causes the counters to be equal. The memory capacity of 16 digits can fully be used if there is at least one read-pulse occurring between the first and the 15th writing pulse.

The memory information will remain after the reading and resetting of the write or read counter.

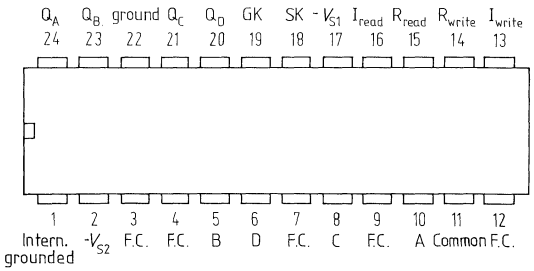
With each writing pulse an information present on the corresponding memory location is replaced. Write or read pulses must overlap with reset pulses possibly occurring at the same time.

Reset, write and read pulses are operating statically (level-effective). The memory condition SK indicates an H-level (corresponding to a logic zero), if after resetting the write and read counter an equal number of write and read pulses has been applied.

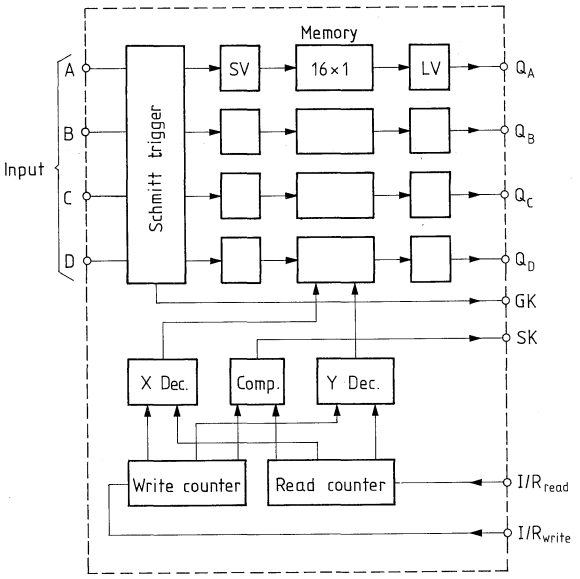
GK (common contact) has a level L (corresponding to a logic 1), if one input (A . . . D) is H.

Even when the read counter remains reset (R_{read} on L-level), new information may be written into the memory.

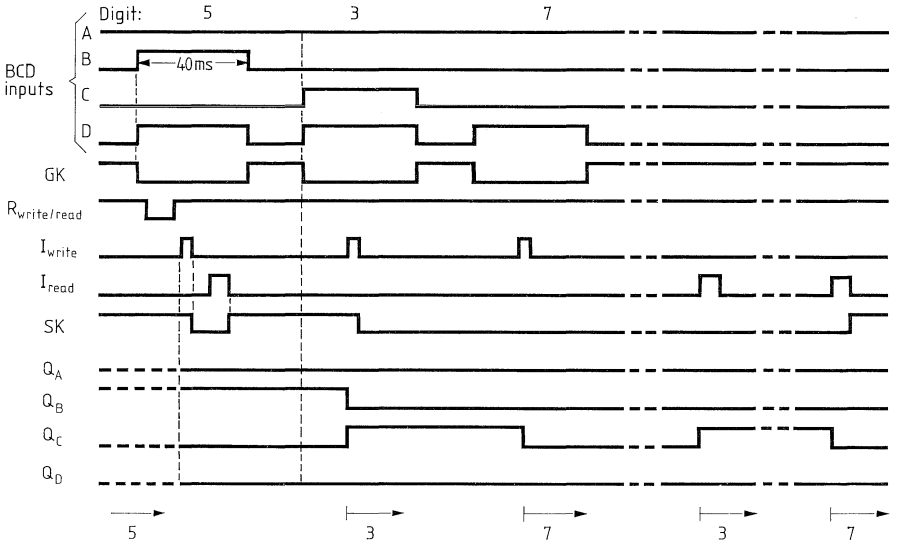
Pin configuration
top view



Block diagram



Timing diagram



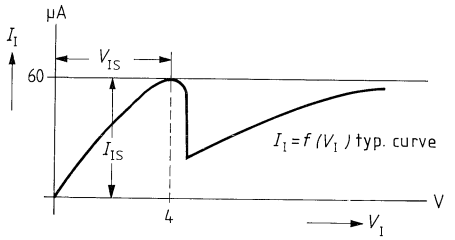
Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage	$V_{S1} = V_{S2}$	−30	0.3	V
Input voltage	V_I	V_{S1}	0.3	V
Output current	$-I_Q$		10	mA
Ambient temperature	T_{amb}	−25	85	°C
Storage temperature	T_s	−55	125	°C
Power dissipation	P_{tot}		400	mW
Load capacitance	C_0		50	pF

Electrical characteristics

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Ambient operating temperature range	T_{amb}				70	°C
Supply current	I_{S1}	outputs unloaded			10	mA
	I_{S2}				1	mA
Supply voltage		$V_{S1} = V_{S2}$, quasistatic, $f_0 = 20.48$ kHz, $t_P = 1$ µs,	−27		−23	V
		$V_{S1} = V_{S2}$	−27		−23	V
Input with Schmitt-trigger		reg. inputs A...D				
H-input voltage	V_{IH}		−2			V
H-input current	I_{IH}	$V_{IH} = -2$ V			150	µA
L-input voltage	V_{IL}		V_{S1}		−9	V
L-input current	I_{IL}	$V_{IL} = -27$ V			250	µA
Input threshold (see figure)	V_{IT}	$I_{IT} \leqq 250$ µA	−8	−4	−3	V
Input without Schmitt-trigger						
H-input voltage	V_{IH}		−2			V
H-input current	I_{IH}	$V_{IH} = -2$ V			10	µA
L-input voltage	V_{IL}	V_{S1}			−9	V
L-input current	I_{IL}	$V_{IL} = -27$ V			10	µA
Outputs Q_A...Q_D						
L-output voltage	V_{QL}	$I_{QL} = 0$	V_{S1}		−10	V
L-output voltage	V_{QL}	$I_{QL} = 100$ µA	V_{S1}		−9	V
H-output voltage	V_{QH}	$I_{QH} = 100$ µA	−1			V

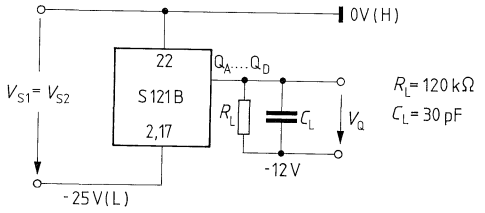
Input current $I_I = f(V_I)$



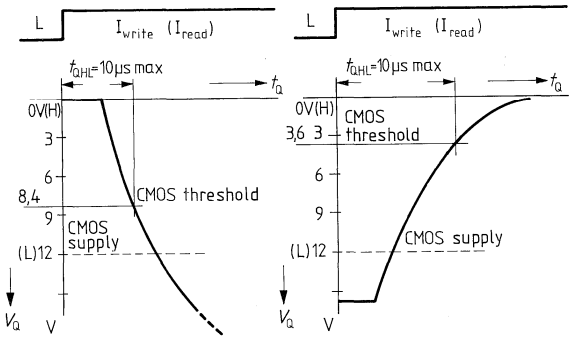
Dynamic characteristics

	Lower limit B	Upper limit A	Unit
Static operation with S 120 A 3			
Input timing			
Inputs A...D	t'_1	20	ms
Contact bounce	τ'_1	6	ms

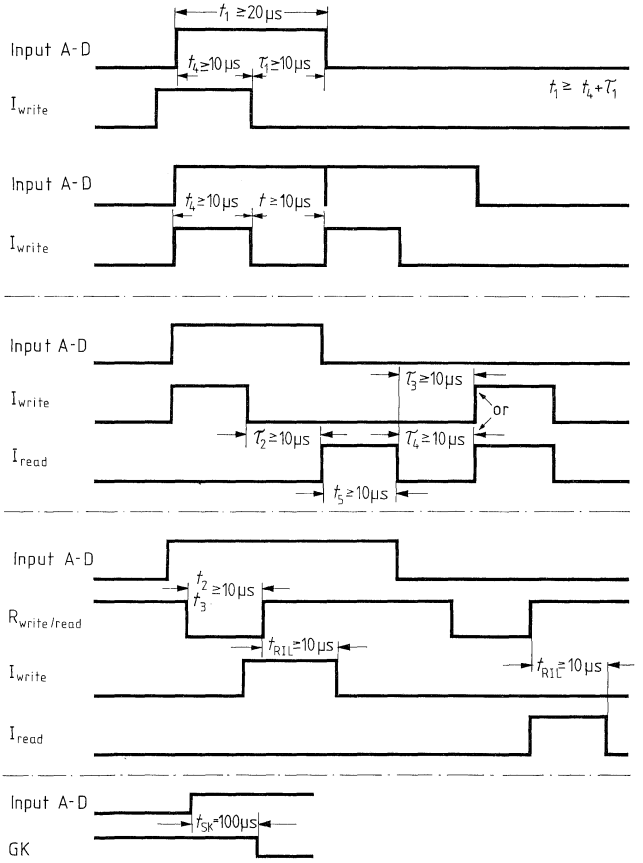
Connection of outputs $Q_A \ldots Q_D$



Output transition timing

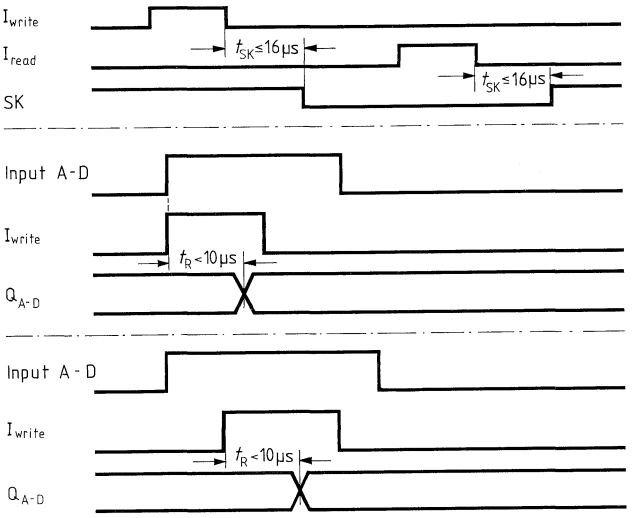


Timing diagram



Time intervals are from 50 % of the first pulse voltage to 50 % of the second pulse voltage.

Timing diagram



Dynamic characteristics

		Lower limit B	Typ.	Upper limit A	Unit
Quasistatic operation with S 120 A 3 f_0 = 20.48 kHz, t_p = 1 µs					
Pulse length Inputs A...D	t_1	20	40		ms
Duration of bounce	τ_1			6	ms

Preliminary data

Type	Ordering code	Package outline
S 359	Q67000–Y477	Figure No. 1

The MFV push-button dialling oscillator S 359 in I^2L-technology generates the MFV frequencies in a 2×1 of 4 code. The precision of the frequency is determined by an external standard quartz (4.194 MHz); therefore, adjustment is not required.

The internal temperature-compensated reference voltage source determines the output level and controls the built-in parallel voltage regulator, which ensures proper adaptation to wiring conditions.

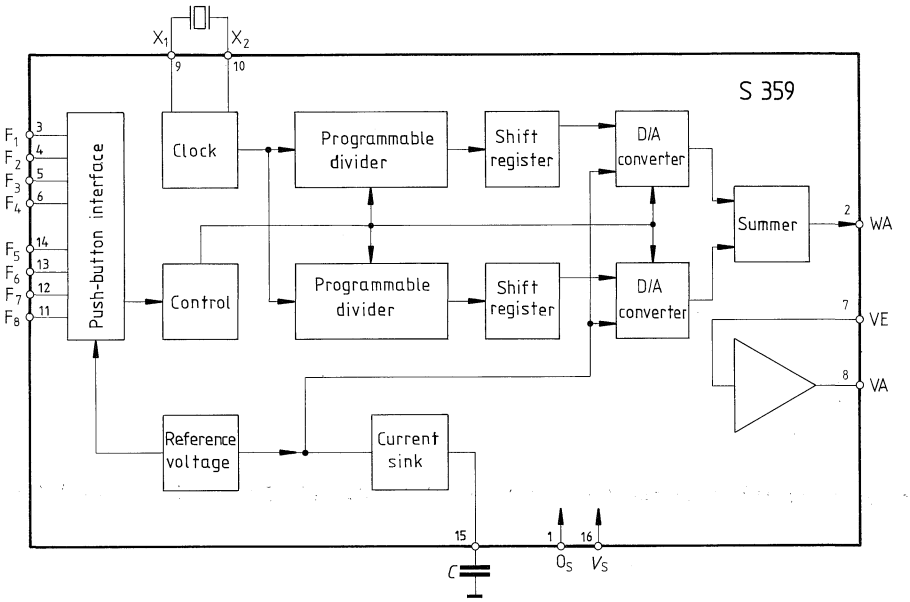
An external 2-pole RC filter can directly be connected in order to meet the CEPT requirements.

The S 359 can be driven by matrix-coded mechanical contacts or open collectors in the push-button code. In addition, BCD control with open collectors is possible.

Features

- CEPT specification complied with
- Direct power supply
- High precision of frequency (better than 0.4 %)
- Cost efficient standard quartz (2^{22} Hz)
- May be operated with BCD or MFV push-button code, as required
- Electronic key-interlock and bounce suppression
- Single frequency also possible
- Thermal limitation of power dissipation

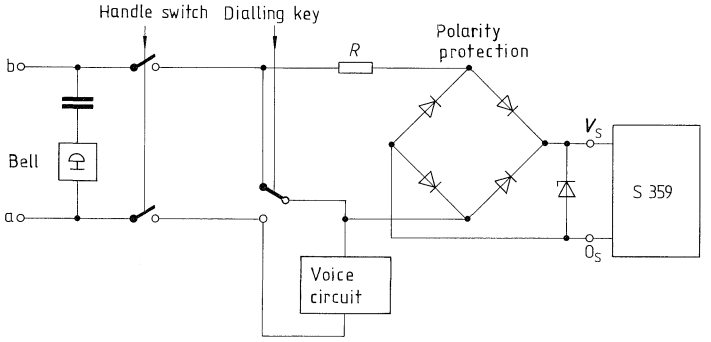
Block diagram and pin configuration



Pin names

O_S, V_S	Supply voltage
F_1–F_8	Coding inputs
X_1–X_2	Connection for quartz $f = 2^{22}$ Hz = 4.194304 MHz
WA	Converter output
VE	Inverting input – output amplifier
VA	Output amplifier
C	Connection of filter capacitor

Connection of push-button dialling oscillator



Technical data

Frequency tolerance

	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	Unit
Required frequency	697	770	852	941	1209	1336	1477	1633	Hz
Actual frequency	697.2	771	851.1	943	1212.6	1337.5	1472.7	1638.4	Hz
Difference	0.275	1.374	–1.037	2.087	3.829	1.1	–2.898	3.307	‰

Maximum ratings

			Lower limit B	Upper limit A	Unit
Supply voltage					
Voltage at all connections	V_S	referred to $O_S = 0$ V	14	–0.3	V
Storage temperature	T_s		–55	125	°C
Ambient temperature	T_{amb}		–25	70	°C

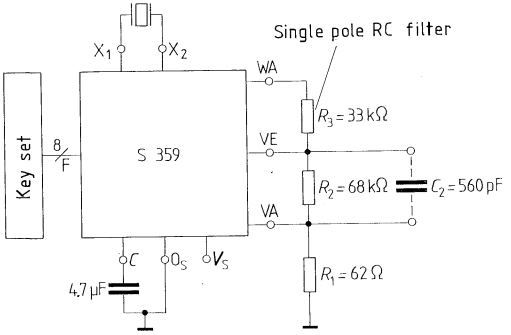
Electrical characteristics

Supply current range:	$12\,mA < I_S < 120\,mA$
(Nominal voltage:	$V_S = 5\,V$)
Voltage supply dependent on wiring	
Internal resistance ($f > 300$ Hz):	$600\Omega < R_I < 1100\Omega$

Levels

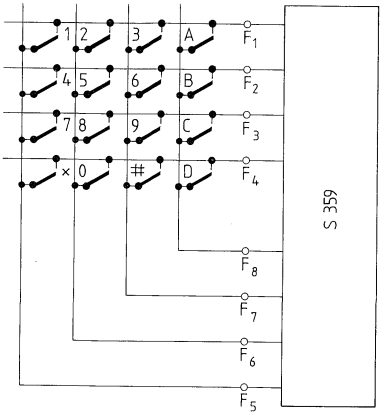
Sum level	$P_S = -4\,dB\,m \pm 2\,dB$
Preemphasis	$P_D = 2\,dB \pm 1\,dB$
Debounce time	$2\,ms < t_E < 6\,ms$

External circuitry for push-button dialling oscillator



VE and VA are the connections of an operational amplifier; between WA, VE, VA, a 2-pole RC filter may be used to meet the CEPT requirements.

Connection of push-button set

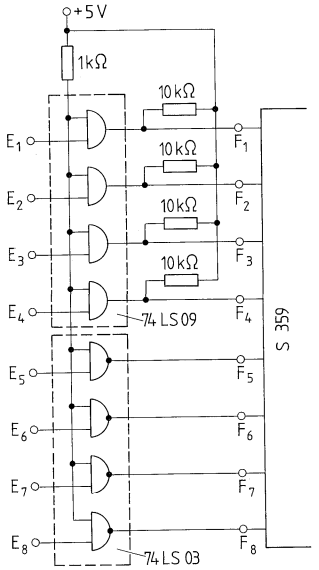


The push buttons are debounced and electronically interlocked. If more than one key is pressed simultaneously, the push buttons recognized as pressed first, will be evaluated.

The requirements for the quality of contacts are:

Open contact:	Shunt resistance $R_N > 50\,k\Omega$
Closed contact:	Contact resistance $R_E \leqq 1\,k\Omega$ for $I = 100\,\mu A$

Electronic control using the push-button code

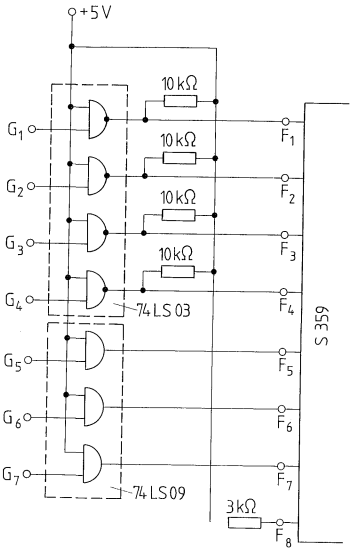


Inputs E_1–E_4 control the frequencies of the lower frequency group f_1–f_4, inputs E_5–E_8 control the frequencies of the upper frequency group f_5–f_8, accordingly. For transmission of a digit, one input E_1–E_4 of the lower group and one input E_5–E_8 of the upper group must be at an H-level. If more than one input within a group is at an H-level, this condition is recognized as a twice pressed push button, and only the first digit recognized is transmitted.

Truth table

E_1	1	2	3	A	Digit
E_2	4	5	6	B	
E_3	7	8	9	C	
E_4	*	0	#	D	
Inputs	E_5	E_6	E_7	E_8	

Electronic control using the BCD code



The push-button information is present at inputs G_1–G_4 in BCD code

Digit		0	1	2	3	4	5	6	7	8	9	X	#	A	B	C	D
Input	G_4	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
	G_3	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
	G_2	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
	G_1	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H

Inputs G_5–G_7 are used as enable inputs

G_5 enable of lower frequency group f_1–f_4

G_6 enable of upper frequency group f_5–f_8

G_7 enable of upper and lower frequency group

H-level blocks the frequencies, L-level enables the frequencies.

Preliminary data

Type	Ordering code	Package outline
SM 301	Q67100–X2	Figure No. 2

Brief description

The MFV Codec Receiver SM 301, fabricated in n-channel technology, processes push-button signals in a 2 × 1 of 4 code according to CCITT recommendation Q 23 with or without accompanying dc signal.

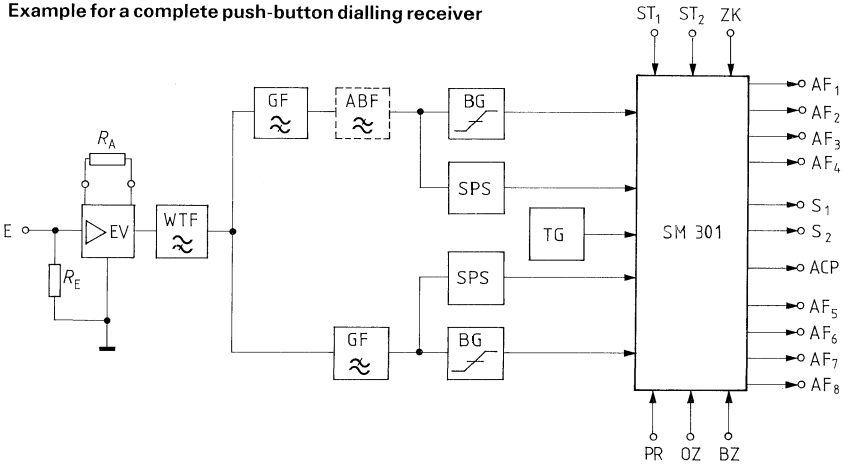
The ac signals present are converted to dc signals. 3 output codes may be chosen.

An analog circuit performs the separation of the 2 signal frequency groups by means of filters, as well as blocking of the dial tone (e.g. for the first digit), conversion of the thus separated signal-frequencies into rectangular pulse signals als well as supplementary voice-protection measures.

Features

- CEPT specification complied with
  voice protection
  noise immunity (signal/noise ratio selectable as 12 dB or 4 dB).
- Cost-efficient standard quartz (2^{22} Hz)
- Digital processing of the MFV signals and conversion into several output codes with scanning 2 × 1 of 4 code
  binary code
  2 of 6 code
  } 16 combinations with carry
- Code control output for information transfer
- Suited for MFV dialling methods (according to CEPT)
  without accompanying dc signal
  with accompanying dc signal
- Mean evaluation time of the SM 301
  without accompanying dc signal approx. 28 ms
  with accompanying dc signal approx. 15 ms (12 to 19 ms)
- 2 splitting outputs for fast separation of the propagating voice paths, even with high noise levels
  Access time of the splitting outputs: S_1 approx. 3 ms, S_2 approx. 15 ms (12 to 19 ms)
- Holding time of the digit output freely selectable by means of external circuits:
  Fixed holding time for by-pass of signal interruptions $\leqq$ 20 ms at input according to CEPT.
  Any holding time desired by means of external timing circuit
  No holding time for higher transfer frequencies up to 20 signals/sec.
- Simple means of adapting to different output interfaces:
  Electronic interface for the following IC families:
  TTL, CMOS, NMOS
  Relay driver with 2 mA input current
- Low power consumption
- 5 V supply

Example for a complete push-button dialling receiver



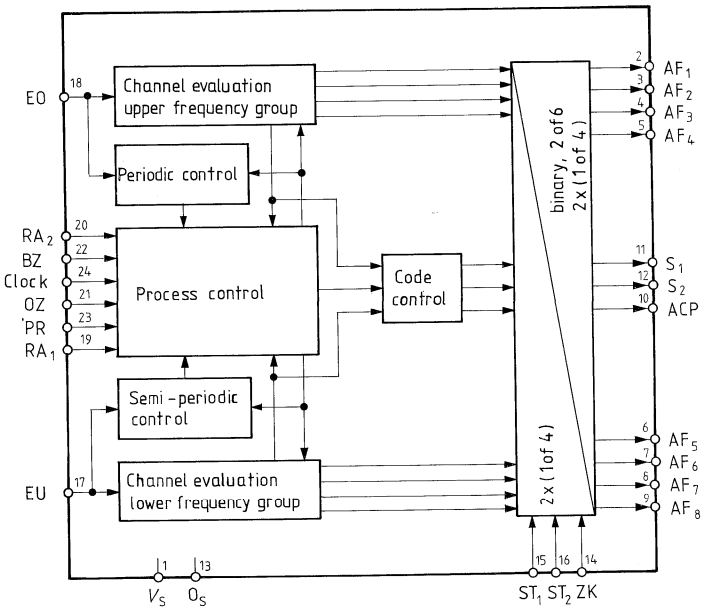
Function blocks

EV	Input amplifier
WTF	Dial tone filter
GF	Group filter
BG	Limiter
SPS	Voice protection circuit
TG	Clock generator
ABF	Out-band filter

Inputs/Outputs

E	Input
EO, EU	Limiter output for upper or lower frequency group, respectively
RA_1, RA_2	Access to voice protection circuits
ST_1, ST_2	Control inputs for output code
ZK	External control of delay time
BZ	Switching of accompanying signal technique
OZ	Switching of output delay prolongation
PR	Switching of noise margin 12 dB/4 dB
$AF_1 \ldots AF_8$	Outputs
ACP	Codec control outputs
S_1, S_2	Splitting outputs

Block diagram



Keyboard Encoder with Buffer

S 600 E 5
S 600 E 5-P

Preliminary data

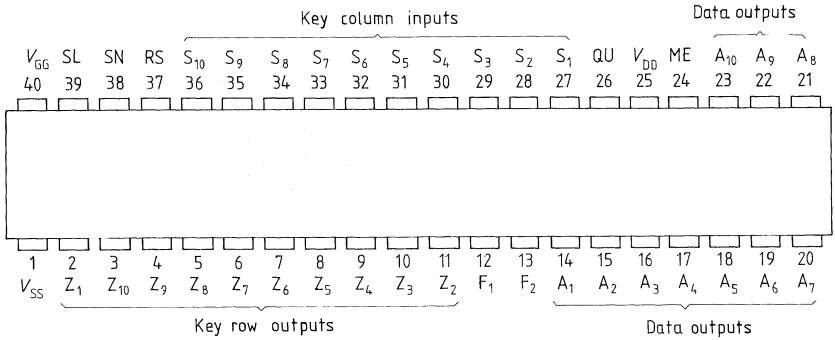
Type	Ordering code	Package outline
S 600 E 5	Q67100-Z101V5	Ceramic/Figure No. 5
S 600 E 5-P	Q67100-Z133V5	Plastic/Figure No. 5

The IC S 600 E5, fabricated in PMOS technology, is suitable for all common keyboards on data input units, for example typewriters, teleprinters, data display stations, etc.

Up to 90 keys in the keyboard, which are arranged electrically to form a matrix, are interrogated cyclically by the IC. When a key is depressed, the corresponding code character is transmitted. The code belonging to the keys can be mask programmed in a ROM in four levels of 90×10 bits each. This means that two different keyboards with triple allocation can be implemented (see pages 281/282). Various control functions can be selected with push buttons or soldering link connectors at ten further points of the matrix.

The S 600 E 5 differs advantageously from other keyboard integrated circuits in that it contains additional contact debounce and an internal buffer for three characters.

Pin configuration,
top view



RS = Reset input
QU = Acknowledge
SN = Blocking input
ME = Message
SL = Shift-lock message
F_1, F_2 = Frequency inputs

Functional overview on the basis of the block diagram

The complete keyboard consists of the keyset with the contact matrix consisting of 10 + 10 lines and the connected keyboard electronics, which are completely integrated in the MOS device.

Depression of a key causes the keyboard electronics to present the corresponding encoded data at the outputs A_1 to A_{10}.

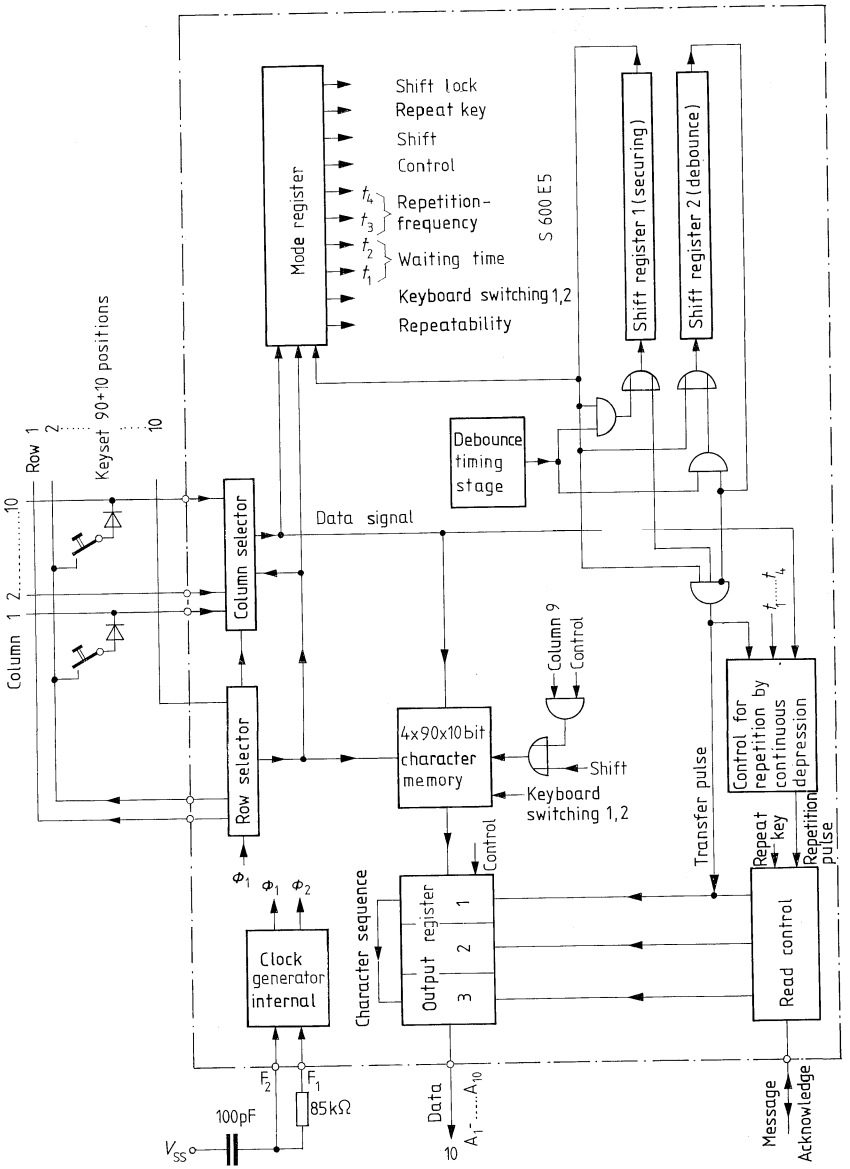
The main parts of the circuit are:

- the **read portion,** consisting of **row selector** and **column selector,** which continuously interrogates the 10 × 10 matrix of the keyset;
- two **shift registers** and one **contact debounce stage,** for suppression of contact bounce and protection against noise;
- the mask programmable **character memory,** which contains the data of 2 × 2 × 90 characters of 10 bits each, and is controlled in synchronism with the read portion;
- the **output registers,** which can buffer up to three characters;
- the **fetch control,** which controls the transfer of characters from the memory to the registers and the output to the interface;
- the **mode register,** which converts up to 10 keys into special functions;
- the **control for repetition of characters by continuous depression**
  A circuit with two timing stages recognizes continuous depression of a key and carries the character releasing pulses to the fetch control after a preset waiting period; repetition rates of 60, 90 and 120 ms can be set depending on the encoding of t_3 and t_4.

The waiting period before repetition, caused by continuous depression of a key, can be set to values of 300, 390, and 480 ms with the aid of t_1 and t_2. If "L" signal is present at t_1 and t_2, repetition by continuous depression of a key is blocked.

- the **control for character sequences,** which generates one of two possible characters and places it in front of the selected character when specific characters flagged in the 10th bit are selected from the character memory. These character sequences can be repeated;
- **changeover to generation of control characters,** by code conversion of the characters coming from the character memory;
- the **clock generator** for generating the 66 kHz internal auxiliary clock signals.

Block diagram



Absolute maximum ratings[1])

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Input voltage	V_I		−20		0.3	V
Supply voltage	V_{DD}		−20		0.3	V
Ambient temperature	T_{amb}		−25		70	°C
Storage temperature	T_s		−55		125	°C
Power dissipation	P_{tot}	$T_{amb} = 25°C$			800	mW
Power dissipation per output	P_Q				0.4	mW

Electrical characteristics (general) $T_{amb} = -25$ to 70° C
All voltages referred to $V_{DD} = 0$ V

Supply voltage	V_{SS}		4.75	5	5.25	V
Supply voltage	$-V_{GG}$		14	12	11	V
Supply current	I_{GG}	$V_{GG} = -12$ V, $V_{SS} = 5$ V			50	mA
Supply current	I_{DD}	$V_{SS} = 5$ V, $V_{GG} = -12$ V, $R_a = 12$ kΩ			10	mA
Input reverse current, $T_{amb} = 25°C$	I_I	$V_I = V_{SS} = -18$ V			5	µA
Input capacitance to V_{SS}	C_I	$V_I = 0$ V, $f = 1$ MHz			50	pF

[1]) Stresses above those listed under "Absolute maximum ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

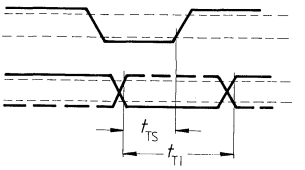
Electrical characteristics (inputs)
All voltages referred to $V_{DD} = 0\,V$

		Remarks	Lower limit B	Typ.	Upper limit A	Unit
Inputs QU, SN, RS						
H-input voltage	V_{IH}		$V_{SS}-1.5$		V_{SS}	V
L-input voltage	V_{IL}		0			V
Stabilizing time	t_{TS}	Pulse diagram 1	2			µs
Pulse width	t_{TI}		4			µs
Signal transition time	t_{THL} }		0.005		0.05	µs
	t_{TLH} }					
Key column inputs $S_1 \ldots S_{10}$						
H-input voltage	V_{IH}		$V_{SS}-2.5$		V_{SS}	V
L-input voltage	V_{IL}		V_{GG}		$V_{SS}-8$	V
Stabilizing time	t_{TS}	Pulse diagram 1	2			µs
Pulse width	t_{TI}		4			µs
Electrical characteristics (outputs)						
Outputs $A_1 \ldots A_{10}$, ME in push-pull mode						
H-output voltage	V_{QH}		$V_{SS}-0.6$		V_{SS}	V
L-output voltage	V_{QL}	$V_{GG} = -11\,V$	0		0.5	V
Delay time	t_D	$V_{SS} = 4.75\,V$			5	µs
		Test circuit 1				
		Pulse diagram 2				
Outputs $A_1 \ldots A_{10}$, ME in tristate mode						
Tristate output voltage in blocking condition	V_{QS}	$V_{GG} = -11\,V$ Pulse diagram 3	1.5		3.5	V
L-output current	I_{QL}				0.4	mA
Delay time	t_{DL}	Test circuit 2, $V_{SS} = 5\,V$		30		µs
Delay time	t_{DH}	Test circuit 1, $V_{SS} = 4.75\,V$			5	µs
Key row outputs $Z_1 \ldots Z_{10}$						
H-output voltage	V_{QH}	$V_{GG} = -11\,V$	$V_{SS}-1$		V_{SS}	V
L-output voltage	V_{QL}	$V_{SS} = 4.75\,V$	V_{GG}		$V_{SS}-9$	V
		Test circuit 3				
Delay time	t_{DLH}	Pulse diagram 4			5	µs
Delay time	t_{DHL}				3.6	µs
Output SL, shift lock						
H-output voltage	V_{QH}	$V_{GG} = -11\,V$	$V_{SS}-2$		V_{SS}	V
L-output voltage	V_{QL}	$V_{SS} = 5\,V$	V_{GG}		$V_{SS}-5$	V
		Test circuit 4				
Delay time	t_D	Pulse diagram 5			6	µs
Signal transition time	t_{THL}				1	µs
	t_{TLH}				1	µs

Pulse diagram 1

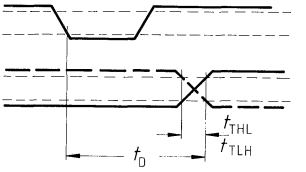
Reference signal:
Clock Φ_2

Input signal V_{IH}
V_{IL}



Pulse diagram 2

Reference signal:
Clock Φ_1

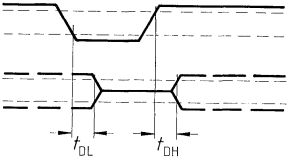


Pulse diagram 3

Reference signal:
Blocking SN

RS = H-signal

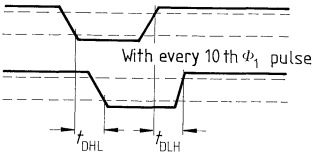
Output signals $A_1 \ldots A_{10}$, ME V_{QH}
V_{QL}



Pulse diagram 4

Reference signal:
Clock Φ_1

Key row outputs $Z_1 \ldots Z_{10}$ V_{QH}
V_{QL}

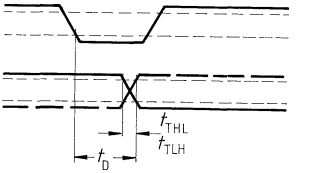


Pulse diagram 5

Reference signal:
Clock Φ_1

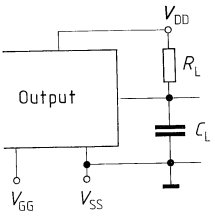
Output signals Shift lock V_{QH}
V_{QL}

Output SL



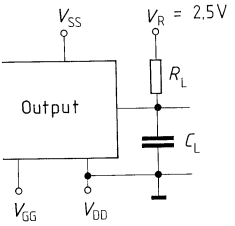
Test circuits

Test circuit 1:



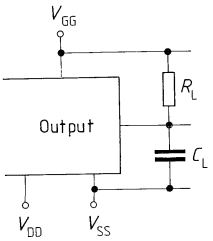
R_L = 50 kΩ. C_L = 40 pF

Test circuit 2:



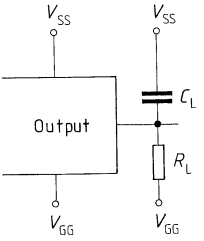
R_L = 50 kΩ. C_L = 40 pF

Test circuit 3:



R_L = 30 kΩ C_L = 170 pF

Test circuit 4:

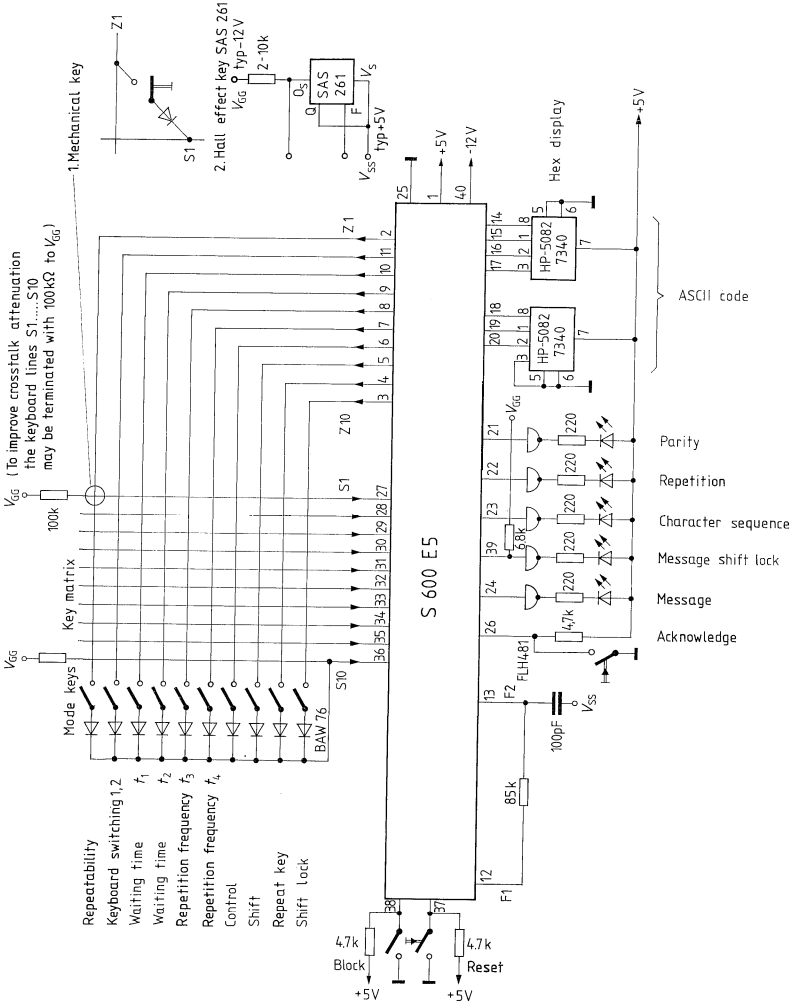


R_L = 6.8 kΩ ±5 %
C_L = 20 pF
I_{LL} = 1.6 mA

Test circuit 5:

In order to test the internal clock generator, twice the operating frequency is applied to F2 (without external RC-network). The resulting Φ_1 clock can be obtained at outputs $Z_1 \ldots Z_{10}$, connected with a ten-input AND gate.

Test circuit S 600 E 5



COLUMN / ROW Key-board matrix		COL ROW code table accord. to CCITT/5		BIT 8	Comment	COL ROW code table accord. to CCITT/5		BIT 8	Comment	CONTROL	BIT 9	BIT 10
		UNSHIFT				SHIFT						
		Allocation I				II				III		
Keyboard 1												
1	1	7	12		FC HEX	7	13		FD HEX		x	x
1	2	7	9	x	y	5	9	x	Y	EM	x	x
1	3	7	5	x	u	5	5	x	U	NAK	x	x
1	4	7	10	x	z	5	10	x	Z	SUB	x	x
1	5	6	14	x	n	4	14	x	N	SO	x	x
1	6	7	7	x	w	5	7	x	W	ETB	x	x
1	7	6	8	x	h	4	8	x	H	BS	x	x
1	8	6	1	x	a	4	1	x	A	SOH	x	x
1	9	6	2	x	b	4	2	x	B	STX	x	x
1	10	7	1	x	q	5	1	x	Q	DC1	x	x
2	1	6	10	x	j	4	10	x	J	LF	x	x
2	2	6	3	x	c	4	3	x	C	ETX	x	x
2	3	7	4	x	t	5	4	x	T	DC4	x	x
2	4	6	4	x	d	4	4	x	D	EOT	x	x
2	5	7	6	x	v	5	6	x	V	SYN	x	x
2	6	6	5	x	e	4	5	x	E	ENQ	x	x
2	7	6	6	x	f	4	6	x	F	ACK	x	x
2	8	7	8	x	x	5	8	x	X	CAN		x
2	9	7	2	x	r	5	2	x	R	DC2	x	x
2	10	7	3	x	s	5	3	x	S	DC3	x	x
3	1	6	7	x	g	4	7	x	G	BEL	x	x
3	2	6	12	x	l	4	12	x	L	FF	x	x
3	3	3	2	x	2	2	2	x	"		x	x
3	4	6	15	x	o	4	15	x	O	SI	x	x
3	5	3	4	x	4	2	4	x	$		x	x
3	6	6	11	x	k	4	11	x	K	VT	x	x
3	7	3	5	x	5	2	5	x	%		x	x
3	8	6	9	x	i	4	9	x	I	HT	x	x
3	9	7	0	x	p	5	0	x	P	DLE	x	x
3	10	2	0	x	SPACE	2	0	x	SPACE		x	x

COLUMN / ROW Key-board matrix		COL ROW code table accord. to CCITT/5		BIT 8	Comment	COL ROW code table accord. to CCITT/5		BIT 8	Comment	CONTROL	BIT 9	BIT 10
		UNSHIFT				SHIFT						
		Allocation I				II				III		
Keyboard 1												
4	1	3	1	x	1	2	1	x	!		x	x
4	2	3	7	x	7	2	7	x	'		x	x
4	3	3	8	x	8	2	8	x	(		x	x
4	4	3	9	x	9	2	9	x	)		x	x
4	5	2	13	x	=	3	13	x	=			x
4	6	6	13	x	m	4	13	x	M	CR	x	x
4	7	2	12	x	,	3	12	x	<		x	x
4	8	3	0	x	O	5	15	x	–	US		x
4	9	3	0	x	O	3	15	x	?			x
4	10	2	14	x	.	3	14	x	>			x
5	1	3	6	x	6	2	6	x	&		x	x
5	2	2	2		A2 HEX	2	3		A3 HEX		x	x
5	3	2	4		A4 HEX	2	5		A5 HEX		x	x
5	4	2	6		A6 HEX	2	7		A7 HEX		x	x
5	5	2	8		A8 HEX	2	9		A9 HEX		x	x
5	6	2	10		AA HEX	2	11		AB HEX		x	x
5	7	2	12		AC HEX	2	13		AD HEX		x	x
5	8	2	14		AE HEX	2	15		AF HEX		x	x
5	9	3	0		B0 HEX	3	1		B1 HEX		x	x
5	10	3	2		B2 HEX	3	3		B3 HEX		x	x
6	1	2	0		A0 HEX	2	1		A1 HEX		x	x
6	2	3	6		B6 HEX	3	7		B7 HEX		x	x
6	3	3	8		B8 HEX	3	9		B9 HEX		x	x
6	4	3	10		BA HEX	3	11		BB HEX		x	x
6	5	3	12		BC HEX	3	13		BD HEX		x	x
6	6	3	14		BE HEX	3	15		BF HEX		x	x
6	7	6	0		E0 HEX	6	1		E1 HEX		x	x
6	8	6	2		E2 HEX	6	3		E3 HEX		x	x
6	9	6	4		E4 HEX	6	5		E5 HEX		x	x
6	10	6	6		E6 HEX	6	7		E7 HEX		x	x

COLUMN	ROW	COL ROW code table accord. to CCITT/5		BIT 8	Comment	COL ROW code table accord. to CCITT/5		BIT 8	Comment	CONTROL	BIT 9	BIT 10
Key-board matrix		UNSHIFT				SHIFT						
		Allocation I				II				III		
Keyboard 1												
7	1	3	4		B4 HEX	3	5		B5 HEX		x	x
7	2	6	10		EA HEX	6	11		EB HEX		x	x
7	3	6	12		EC HEX	6	13		ED HEX		x	x
7	4	6	14		EE HEX	6	15		EF HEX		x	x
7	5	7	0		F0 HEX	7	1		F1 HEX			x
7	6	7	2		F2 HEX	7	3		F3 HEX			x
7	7	7	4		F4 ESC	7	5		F5 ESC		x	
7	8	7	6		F6 ESC	7	7		F7 ESC		x	
7	9	7	8		F8 ESC	7	9		F9 ESC		x	
7	10	0	10	x	NL CRLF	0	10	x	NL CRLF		x	
8	1	6	8		E8 HEX	6	9		E9 HEX		x	x
8	2	3	3	x	3	4	0	x	§	NUL	x	x
8	3	2	15	x	/	6	0	x	'		x	x
8	4	7	13	x	ü	5	13	x	Ü	GS	x	x
8	5	2	11	x	+	2	10	x	*		x	x
8	6	7	12	x	ö	5	12	x	Ö	FS	x	x
8	7	7	11	x	ä	5	11	x	Ä	ESC	x	x
8	8	2	3	x	#	5	14	x	^	RS	x	x
8	9	3	11	x	;	3	10	x	:		x	x
8	10	7	14	x	–	5	15	x	_	US		x
9	1	7	10		FA HEX	7	11		FB HEX		x	x
9	2	3	3	x	3	2	3	x	#		x	x
9	3	5	14	x	^	7	14	x	–	RS	x	x
9	4	4	0	x	@	6	0	x	\	NUL	x	x
9	5	5	11	x	[	7	11	x	{	ESC	x	x
9	3	3	11	x	;	2	11	x	+		x	x
9	7	3	10	x	:	2	10	x	*		x	x
9	8	5	13	x	]	7	13	x	}	GS	x	x
9	9	5	12	x	\	7	12	x	|	FS	x	x
9	10	2	15	x	/	3	15	x	?		x	x

COLUMN / ROW Key-board matrix		COL ROW code table accord. to CCITT/5		BIT 8	Comment	COL ROW code table accord. to CCITT/5		BIT 8	Comment	CONTROL	BIT 9	BIT 10
		UNSHIFT				SHIFT						
		Allocation I				II				III		
Keyboard 2												
0	1	5	0		D0 HEX	5	1		D1 HEX			x
1	2	7	9	x	y	5	9	x	Y	EM		x
1	3	7	5	x	u	5	5	x	U	NAK		x
1	4	7	10	x	z	5	10	x	Z	SUB		x
1	5	6	14	x	n	4	14	x	N	SO		x
1	6	7	7	x	w	5	7	x	W	ETB		x
1	7	6	8	x	h	4	8	x	H	BS		x
1	8	6	1	x	a	4	1	x	A	SOH		x
1	9	6	2	x	b	4	2	x	B	STX		x
1	10	7	1	x	q	5	1	x	Q	DC1		x
1	1	6	10	x	j	4	10	x	J	LF		x
2	2	6	3	x	c	4	3	x	C	ETX		x
2	3	7	4	x	t	5	4	x	T	DC4		x
2	4	6	4	x	d	4	4	x	D	EOT		x
2	5	7	6	x	v	5	6	x	V	SYN		x
2	6	6	5	x	e	4	5	x	E	ENQ		x
2	7	6	6	x	f	4	6	x	F	ACK		x
2	8	7	8	x	x	5	8	x	X	CAN		x
2	9	7	2	x	r	5	2	x	R	DC2		x
2	10	7	3	x	s	5	3	x	S	DC3		x
2	1	6	7	x	g	4	7	x	G	BEL		x
3	2	6	12	x	l	4	12	x	L	FF		x
3	3	3	2	x	2	2	2	x	"			x
3	4	6	15	x	o	4	15	x	O	SI		x
3	5	3	4	x	4	2	4	x	S			x
3	6	6	11	x	k	4	11	x	K	VT		x
3	7	3	5	x	5	2	5	x	%			x
3	8	6	9	x	i	4	9	x	I	HT		x
3	9	7	0	x	p	5	0	x	P	DLE		x
3	10	2	0	x	SPACE	2	0	x	SPACE			x

COLUMN / ROW		COL ROW code table accord. to CCITT/5		BIT 8	Comment	COL ROW code table accord. to CCITT/5		BIT 8	Comment	CONTROL	BIT 9	BIT 10
Key-board matrix		UNSHIFT				SHIFT						
		Allocation I				II				III		
Keyboard 2												
3	1	3	1	x	1	2	1	x	!			x
4	2	3	7	x	7	2	15	x	/			x
4	3	3	8	x	8	2	8	x	(			x
4	4	3	9	x	9	2	9	x	)			x
4	5	7	14	x	ß	3	15	x	?			x
4	6	6	13	x	m	4	13	x	M	CR		x
4	7	2	12	x	,	3	11	x	;			x
4	8	5	2		D2 HEX	5	3		D3 HEX		x	x
4	9	3	0	x	0	3	13	x	=			x
4	10	2	14	x	.	3	10	x	:			x
4	1	3	6	x	6	2	6	x	&			x
5	2	2	2		A2 HEX	2	3		A3 HEX			
5	3	2	4		A4 HEX	2	5		A5 HEX			
5	4	2	6		A6 HEX	2	7		A7 HEX			
5	5	2	8		A8 HEX	2	9		A9 HEX			
5	6	2	10		AA HEX	2	11		AB HEX			
5	7	2	12		AC HEX	2	13		AD HEX			
5	8	2	14		AE HEX	2	15		AF HEX			
5	9	3	0		B0 HEX	3	1		B1 HEX			
5	10	3	2		B2 HEX	3	3		B3 HEX			
5	1	2	0		A0 HEX	2	1		A1 HEX		x	x
6	2	3	6		B6 HEX	3	7		B7 HEX		x	
6	3	3	8		B8 HEX	3	9		B9 HEX		x	
6	4	3	10		BA HEX	3	11		BB HEX		x	
6	5	3	12		BC HEX	3	13		BD HEX		x	
6	6	3	14		BE HEX	3	15		BF HEX		x	
6	7	6	0		E0 HEX	6	1		E1 HEX		x	
6	8	6	2		E2 HEX	6	3		E3 HEX		x	
6	9	6	4		E4 HEX	6	5		E5 HEX		x	
6	10	6	6		E6 HEX	6	7		E7 HEX		x	

COLUMN / ROW Key-board matrix		COL ROW code table accord. to CCITT/5		BIT 8	Comment	COL ROW code table accord. to CCITT/5		BIT 8	Comment	CONTROL	BIT 9	BIT 10
		UNSHIFT				SHIFT						
		Allocation I				II				III		
Keyboard 2												
6	1	3	4		B4 HEX	3	5		B5 HEX		x	
7	2	6	10		EA HEX	6	11		EB HEX		x	
7	3	6	12		EC HEX	6	13		ED HEX		x	
7	4	6	14		EE HEX	6	15		EF HEX		x	
7	5	7	0		F0 HEX	7	1		F1 HEX		x	
7	6	7	2		F2 HEX	7	3		F3 HEX		x	
7	7	7	4		F4 HEX	7	5		F5 HEX		x	
7	8	7	6		F6 HEX	7	7		F7 HEX		x	
7	9	7	8		F8 HEX	7	9		F9 HEX		x	
7	10	7	10		FA HEX	7	11		FB HEX			x
7	1	6	8		E8 HEX	6	9		E9 HEX		x	
8	2	3	3	x	3	4	0	x	§	NUL		x
8	3	2	7	x	'	6	0	x	'			x
8	4	7	13	x	ü	5	13	x	Ü	GS		x
8	5	2	11	x	+	2	10	x	*			x
8	6	7	12	x	ö	5	12	x	Ö	FS		x
8	7	7	11	x	ä	5	11	x	Ä	ESC		x
8	8	2	3	x	#	5	14	x	^	RS		x
8	9	3	12	x	<	3	14	x	>			x
8	10	2	13	x	–	5	15	x	–	US		x
8	1	7	12		FC HEX	7	13		FD HEX			x
9	2	7	14		FE HEX	7	15		FF HEX			x
9	3	4	0		C0 HEX	4	1		C1 HEX			x
9	4	4	2		C2 HEX	4	3		C3 HEX			x
9	5	4	4		C4 HEX	4	5		C5 HEX			x
9	6	4	6		C6 HEX	4	7		C7 HEX			x
9	7	4	8		C8 HEX	4	9		C9 HEX			x
9	8	4	10		CA HEX	4	11		CB HEX			x
9	9	4	12		CC HEX	4	13		CD HEX			x
9	10	4	14		CE HEX	4	15		CF HEX			x

Bit 8 corresponds to L-signal
Bit 9 is x: No repetition
Bit 10 is x: No character sequence

7-bit code in accordance with JSO/CCITT No. 5

Bits b_7	b_6	b_5	b_4	b_3	b_2	b_1	Row \ Column	0	0	0	0	1	1	1	1
								0	0	1	1	0	0	1	1
								0	1	0	1	0	1	0	1
								0	1	2	3	4	5	6	7
			0	0	0	0	0	NUL	(TC 7) DLE	SP	0	@(§)	P	‘	p
			0	0	0	1	1	(TC 1) SOH	DC 1	!	1	A	Q	a	q
			0	0	1	0	2	(TC 2) STX	DC 2	"	2	B	R	b	r
			0	0	1	1	3	(TC 3) ETX	DC 3	#(£)*	3	C	S	c	s
			0	1	0	0	4	(TC 4) EOT	DC 4	$	4	D	T	d	t
			0	1	0	1	5	(TC 5) ENQ	(TC 8) NAK	%	5	E	U	e	u
			0	1	1	0	6	(TC 6) ACK	(TC 9) SYN	&*	6	F	V	f	v
			0	1	1	1	7	BEL	(TC10) ETB	·	7	G	W	g	w
			1	0	0	0	8	FE 0 (BS)	CAN	(	8	H	X	h	x
			1	0	0	1	9	FE 1 (HT)	EM	)	9	I	Y	i	y
			1	0	1	0	10	FE 2 (LF)	SUB	·	:	J	Z	j	z
			1	0	1	1	11	FE 3 (VT)	ESC	+	;	K	[(Ä)*	k	{(ä)*
			1	1	0	0	12	FE 4 (FF)	IS 4 (FS)	,	<	L	/(Ö)*	l	|(ö)*
			1	1	0	1	13	FE 5 (CR)	IS 3 (GS)	–	=	M	](Ü)*	m	}(ü)*
			1	1	1	0	14	SO	IS 2 (RS)	.	>	N	^*	n	¯(ß)*
			1	1	1	1	15	SI	IS 1 (US)	/	?	O	_	o	DEL

*) National character, in this case assigned in accordance with DIN 66003

Meanings of the abbreviations of equipment and transmission control characters

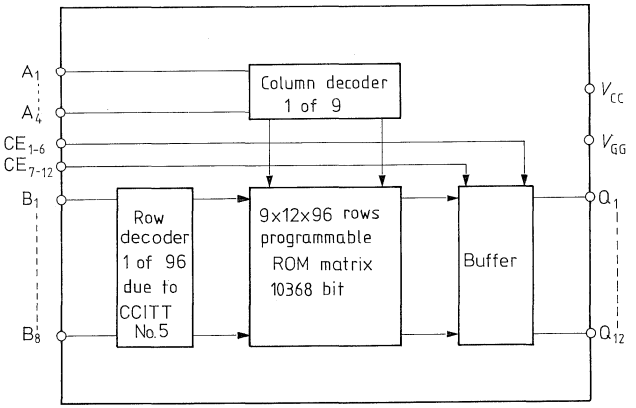
Abbre-viation	Position Column/row	German designation (in accordance with DIN 66003)	International designation
ACK	0/6	Positive Rückmeldung	Acknowledge
BEL	0/7	Klingel	Bell
BS	0/8	Rückwärtsschritt	Backspace
CAN	1/8	Ungültig	Cancel
CR	0/13	Wagenrücklauf	Carriage Return
DC1..4	1/1..1/4	Gerätesteuerung	Device Control
DEL	7/15	Löschen	Delete
DLE	1/0	Datenübertragungs-umschaltung	Data Link Escape
EM	1/9	Ende der Aufzeichnung	End of Medium
ENQ	0/5	Stationsaufforderung	Enquiry
EOT	0/4	Ende der Übertragung	End of Transmission
ESC	1/11	Umschaltung	Escape
ETB	1/7	Ende des Datenübertragungs-blocks	End of Transmission Block
ETX	0/3	Ende des Textes	End of Text
FE	0/8..0/13	Formatsteuerung	Format Effector
FF	0/12	Formularvorschub	Form Feed
FS	1/12	Hauptgruppen-Trennung	File Separator
GS	1/13	Gruppen-Trennung	Group Separator
HT	0/9	Horizontal-Tabulator	Horizontal Tabulation
IS	1/12..1/15	Informationstrennung	Information Separator
LF	0/10	Zeilenvorschub	Line Feed
NAK	1/5	Negative Rückmeldung	Negative Acknowledge
NUL	0/0	Null	Nil
RS	1/14	Untergruppen-Trennung	Record Separator
SI	0/15	Rückschaltung	Shift-in
SO	0/14	Dauerumschaltung	Shift-out
SOH	0/1	Anfang des Kopfes	Start of Heading
SP	2/0	Zwischenraum	Space
STX	0/2	Anfang des Textes	Start of Text
SUB	1/10	Substitution	Substitute Character
SYN	1/6	Synchronisierung	Synchronous Idle
TC	0/1 and others	Übertragungssteuerung	Transmission Control
US	1/15	Teilgruppen-Trennung	Unit Separator
VT	0/11	Vertikal-Tabulator	Vertical Tabulation

Preliminary data

Type	Ordering code	Package outline
S 607	Q67100–Z108	Figure No. 4

Technical characteristics

- p-MOS technology with ion implantation
- Supply voltages +5, –12.0 V
- Static inputs, TTL-compatible
- Tristate outputs
- Maximum output current loading 1.6 mA, typ. 0.4 mA
- Access time approximately 10 µs
- Power dissipation max. 700 mW
- Operating temperature: 0 to 70° C
- Mask-programmable



PCM 2-Channel Codec

SM 61 A
S 291

Preliminary data

Type	Ordering code	Package outline
SM 61 A	Q67100-Z134	Figure No. 3
S 291	Q67000-A1388	Figure No. 2

The PCM 2-channel Codec consists of two ICs, SM 61 A in NMOS technology and S 291 in bipolar technologgy. The favorable characteristics of both technologies permit construction of a PCM system with only a few additional passive components.

Features

- A-companding to CCITT G. 711
- Serial PCM interface 2.048 MHz for 1 PCM 30/32 system
- All digital interfaces TTL compatible
- The PCM is switched on directly by external channel pulse control
- Free selection of the Codec channel in relation to the PCM connection (multiplex system)
- Single stage Codec configuration can be switched directly
- Reading and writing of the PCM information as required and independent of each other
- Codec for 1 or 2 analog channels with 8 kHz sampling or for 1 analog channel with 16 kHz sampling

Applications

- Transmission systems
- Switching systems
- Multiplex terminals
- Digital subscriber circuit
- Single stage concentrator (32 switch channels)
- Single stage switching matrix for PABX and PAX telephone systems (32 switched channels)

Short description

The PCM 2-channel Codec is a configuration for full duplex operation of two independent four-wire telephone circuits (bandwidth <4 kHz, sampling rate 8 kHz). The transmitting and receiving filters, a holding capacitor, and an offset and compensation network are required as external components.

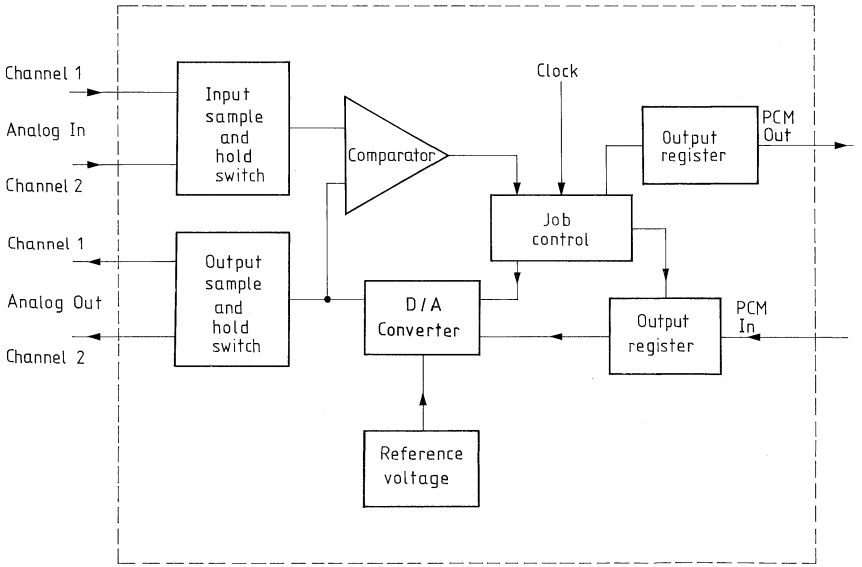
For every analog circuit the PCM information can be connected as required in both directions by external pulse control and independently of the PCM converter to a serial PCM 2.048 MHz multiplex system. This is made possible by a buffer arrangement between the PCM system and the PCM converter.

The Codec can be used without modification as a single channel converter for full duplex operation with a sampling rate of 16 kHz.

Level adjustment for the transmitting and receiving directions is carried out outside the Codec at the filters; the maximum drive limit of the Codec can be adjusted at the compensation network.

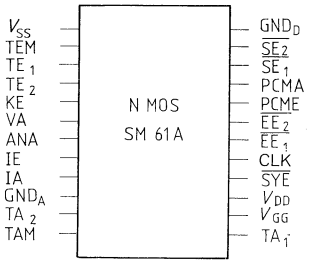
The bipolar chip contains a reference current source, whose polarity can be reversed externally, for D/A conversion, and a current-voltage converter, together with a comparator and two operational amplifiers for flexible matching of the analog inputs. The NMOS chip contains all other necessary components of a PCM Codec, such as coding and decoding sequence control, PCM registers with D/A converters, offset control output, and the buffer arrangement for variable PCM input and output and the input and output sample and hold switches of the analog side.

Block diagram

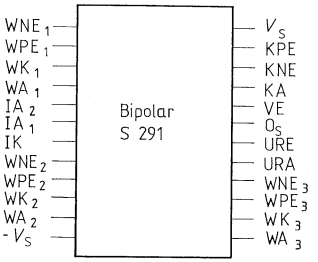


Pin configurations

NMOS SM 61 A



Bipolar S 291



Pin definitions SM 61 A

Symbol	Function	Description
1. Power supplies		
V_{GG}	+12 V ±5%	referred to digital ground, power consumption 150 mW
V_{DD}	+5 V ±5%	
V_{SS}	−5 V ±5%	
GND_D	Digital ground	
CLK	2.048 MHz clock	Duty cycle 1:1
2. Analog interface		
TE_1	2 input sensor, connected on one side	Analog channel 1
TEM		Center point
TE_2		Analog channel 2
GND_A	Analog ground	
TA_1	2 output sensor, connected on one side	Analog channel 1
TAM		Center point
TA_2		Analog channel 2
3. PCM interface		
PCMA	PCM output	PCM information in nini code (even numbered bits inverted), serially at 2.048 MHz. Bit sequence in order to decreasing significance. Channel allocation determined by transmit control pulse $\overline{SE1} + \overline{SE2}$ (otherwise tristate)

Pin definitions SM 61 A

Symbol	Function	Description
PCME	PCM input	PCM information in nini code, serially at 2.048 MHz; channel allocation determined by receiver control pulse $\overline{EE_1} + \overline{EE_2}$

4. External control pulses

Duration of all control pulses corresponds to the channel division of the multiplex system (8 bits). The pulses start with a positive pulse edge and are active at ground potential.

$\overline{SYE}$	Synchronization pulse for PCM converter	Start and synchronization of the PCM converter control. PCM transfer in both directions between PCM converter registers and buffers.
$\overline{EE_1}$ $\overline{EE_2}$	Receiver pulse for analog circuits 1 and 2, respectively	Control pulse for reading the PCM information from the multiplex system into the corresponding PCM buffer for analog circuit 1 and 2, pulse duration 8 clock pulses (corresponding to time sequence).
$\overline{SE_1}$ $\overline{SE_2}$	Transmitter pulse for analog circuits 1 and 2, respectively	Control pulse for writing the PCM information into the multiplex system from the corresponding PCM buffer of the analog circuit 1 or 2, pulse duration 8 clock pulses (corresponding to time sequence).

Pin definitions S 291

Symbol	Function	Description
1. Supply voltages		
V_S	+5 V ±5%	Power consumption 50 mW
O_S	Ground	
$-V_S$	–5 V ±5%	
2. Reference current source		
URA	Reference voltage output	URA = 1.25 V, temperature compensated
URE	Reference current source input	A resistor between URA and URE determines the reference current
IA_1 IA_2	Reference current source output	$IA_1 = -IA_2$
IK	Reference current source compensation	
VE	Input of sign information (TTL compatible)	H-level: $IA_1 > 0$ L-level: $IA_1 < 0$

Pin definitions S 291

Symbol	Function	Description
3. Comparator		
KNE	Inverting input	
KPE	Non-inverting input	
KA	Output	
4. Operational amplifiers		
WNE_1	Inverting inputs of op amps 1, 2, 3	
WNE_2		
WNE_3		
WPE_1	Non-inverting inputs of op amps 1, 2, 3	
WPE_2		
WPE_3		
WA_1	Outputs of op amps 1, 2, 3	
WA_2		
WA_3		
WK_1	Compensation of op amps 1, 2, 3	
WK_2		
WK_3		

Pin definitions MOS/bipolar

1. Signals		
KE	Comparator	Input of comparator decision
VA	Sign	Switched polarity
ANA	Automatic zero balance	Compensates the offset of the comparator
IE	Reference current	Polarity switched by VA
IA	Weighting current D/A	

Maximum ratings

NMOS circuit SM 61 A

Supply voltage (referred to V_{SS})		±20	V
Functional range		$V_{nominal}$ ±10%	V
Ambient temperature	T_{amb}	–25 to 75	°C
Storage temperature	T_s	–60 to 150	°C
Total power dissipation	P_{tot}	300	mW

Bipolar circuit S 291

Supply voltage	V_S	±10	V
Output current	I_{WA}	±30	mA
Differential input voltage	V_{WDE}	±8	V
Input voltage for op amps and comparator		±10	V
for sign		±0.4 to ±10	V
Functional range		±4 to ±10	V
Ambient temperature	T_{amb}	–25 to 75	°C
Junction temperature	T_j	125	°C
Thermal resistance	R_{thsamb}	120	K/W
Total power dissipation	P_{tot}	600	mW
Storage temperature	T_s	–65 to 150	°C

Electrical characteristics

($V_{SS} = -V_S = -5\,V$, $V_{DD} = +V_S = +5\,V$, $V_{GG} = +12\,V$, $T_{amb} = 25°\,C$)

NMOS circuits SM 61 A

Analog value range	±2.5 max.	V
Input level	TTL compatible	
Output level	1 TTL load 200	pF
Input and output capacitance	10 max.	pF
Lowest step sequence	1.2	mV
Autozero	0.4 max.	mV
Output delay time	100	ns
Input hold time	100	ns
Time difference between CLK and $\overline{SYE}$	±50	ns
Resistance of sampling switch	200 Ω; 20 MΩ	
Cross talk attenuation	80	dB

Bipolar circuit S 291

		Min.	Typ.	Max.	Unit
Reference current source					
Reference voltage	V_{RA}	1.2	1.25	1.3	V
Temperature coefficient of V_{RA}	α_{RA}			300	$ppmK^{-1}$
Input offset voltage	V_{ZE}			±5	mV
Impedance of reference current outputs	R_{IA1}		10		MΩ
	R_{IA2}		10		MΩ
Signs					
Input current ($V_{VE} = 0$)	$-I_{VE}$		3	10	µA
H-input voltage	V_{VEH}	2			V
L-input voltage	V_{VEL}			0.8	V

Electrical characteristics (Continued)

Comparator

		Min.	Typ.	Max.	Unit
Input current	I_{KE}		10	50	nA
Input offset voltage	V_{KE}			±5	mV
H-output current	I_{KAH}	200			µA
L-output current	I_{KAL}			10	mA
H-output voltage	V_{KAH}	4			V
L-output voltage	V_{KAL}			–4	V
Hysteresis	V_{KEHY}		0.25	0.4	mV
Voltage gain	A_V		100		dB
Propagation delay	t_{PLH}		0.8		µs
Input common-mode range		±3			V

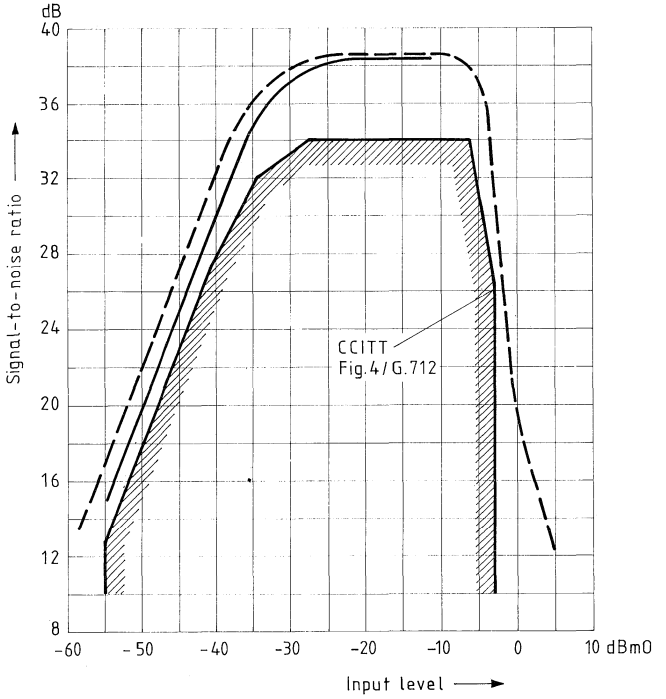
Operational amplifier

Input offset voltage	V_{WEOS}			±5	mW
Input current	I_{WE}		10	30	nA
Input offset current	I_{WEOS}			10	nA
Modulation range ($R_L = 150\,\Omega$)	V_{WA}	–2.5		2.5	V
Input synchronization range	V_{WEG}	–25		2.5	V
Voltage gain	A_V		75		dB
Transient response of an output voltage (1 % error, inverter with $A_V = 0$ dB, voltage variation $V_E = 20$ mV)	t_r		0.5		µs
Leading edge	dV_{WA}/dt		2		V/µs

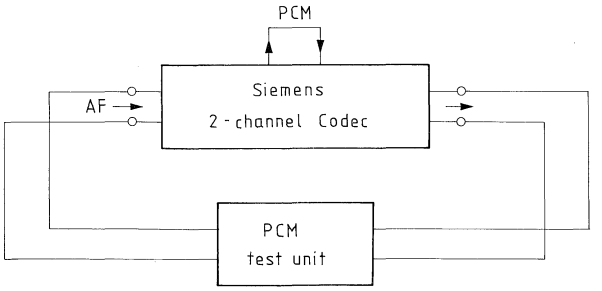
Codec SM 61 A/S 291 System

Signal-to-noise ratio	*S/N*	2 dB above tolerance range	dB
Level dependency of residual attenuation		Within limits of tolerance range	dB
Frequency dependency of residual attenuation		Within limits of tolerance range	dB
Quiescent noise		> –65	dB mO
Cross talk			
Within channel			dB mO
Between channel		> –65	dB mO
Clock frequency		2.048	MHz
Power consumption	P_{tot}	250	mW

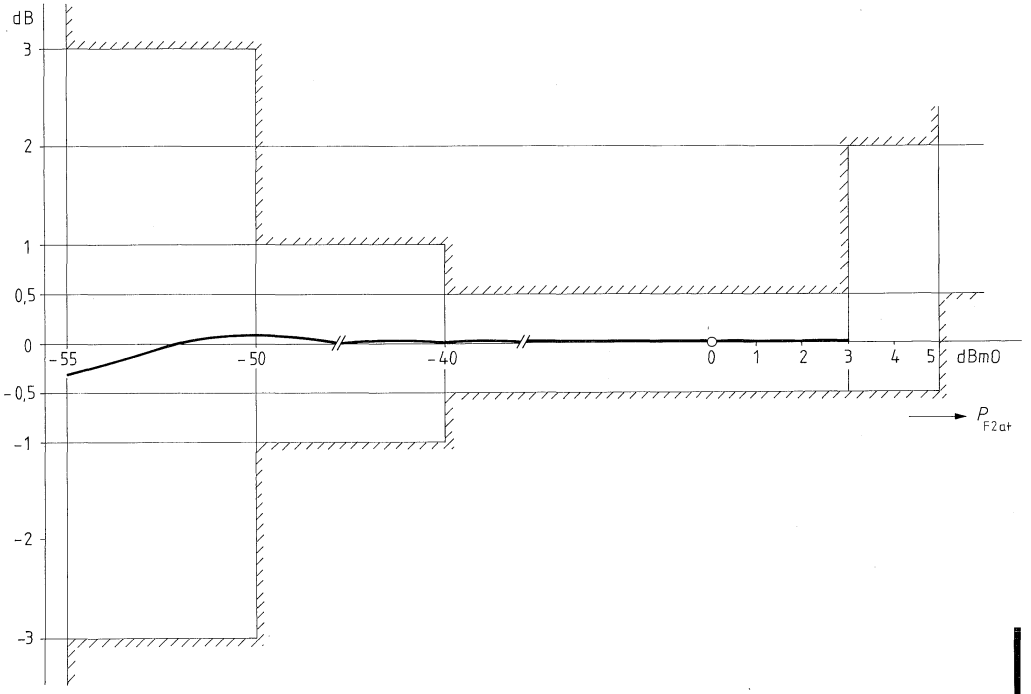
Signal-to-noise ratio in accordance with CCITT



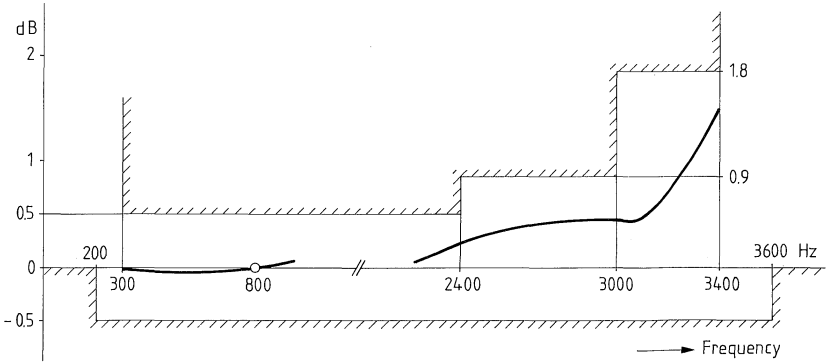
----- Theoretical value
——— Measured curve
Recommended S/D tolerance scheme (CCITT)



Level dependency of residual attenuation



Frequency dependency of the attenuation

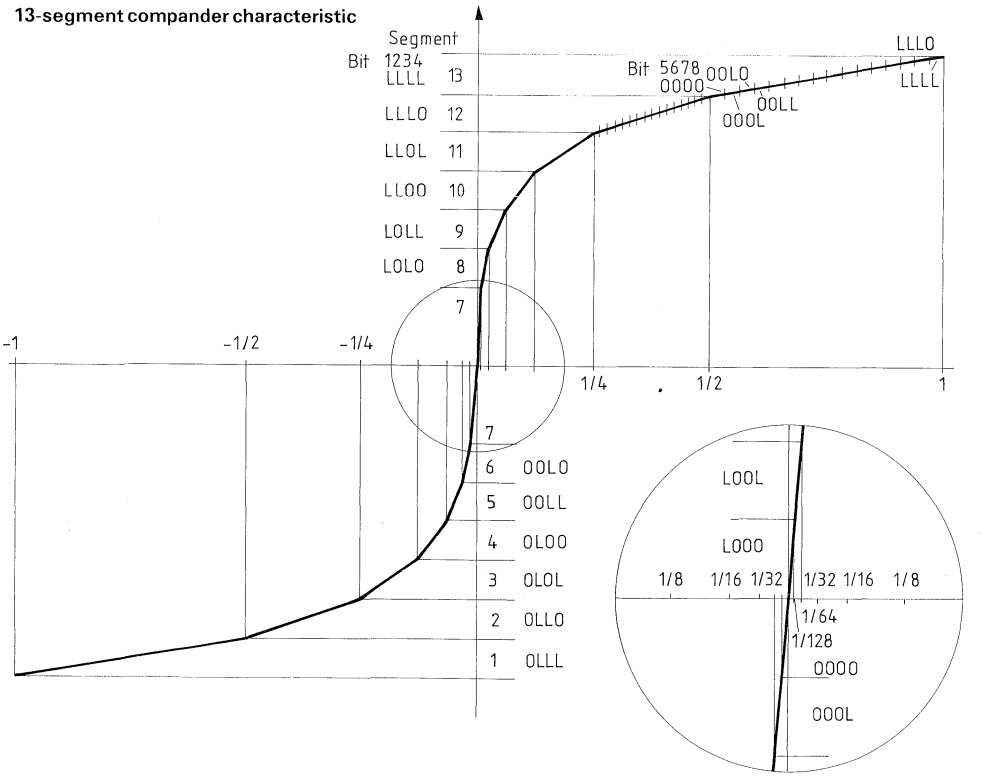


Functional description

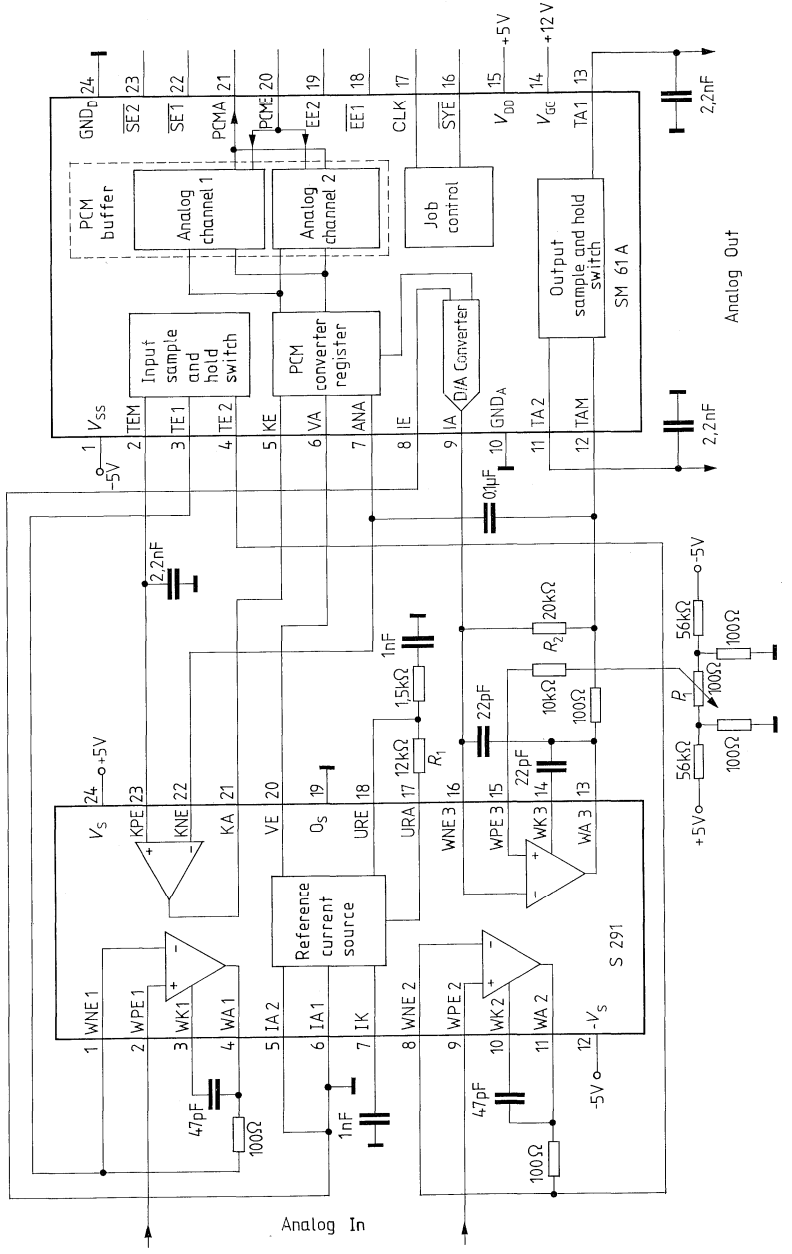
General

In pulse code modulation transmission systems, the low frequency signal mixture, limited by a band-pass filter, is sampled at 8 kHz and converted into an 8-bit PCM code, corresponding to 256 quantization steps. Consequently, coding and decoding with two channels must be executed in the SIEMENS Codec within the clock period of 1/8 kHz = 125 µs. The time multiplex system PCM 30/32 specified by CCITT, using a bit rate of 2.048 Mbit/s, therefore permits nesting of 30 telephone channels and 2 control channels.
CCITT (G. 711) specifies a 13-segment companding characteristic for the analog value and PCM code correlation (A companding), with which the SIEMENS 2-channel Codec conforms. The first bit is determined by the sign of the signal. The 2nd to 4th bits indicate in which of the eight characteristic segments the signal is located. Finally, the last four bits (Bit 5 . . . Bit 8) define one of 16 intervals within the characteristic segment which represents the closest approximation to the sampled value. As the four sections which lie around the zero point have the same rate of increment, and consequently the same resolution (Segment 7), there are 13 segments in the total characteristic with rates of increment in the ratio 2:1, producing a correspondingly higher resolution for small signal amplitudes than for large amplitudes.

13-segment compander characteristic



External circuitry for SM 61 A and S 291

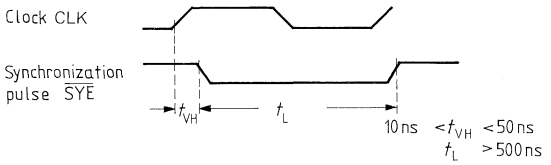


The offset voltage of the current-voltage converter must be adjusted with potentiometer P_1.

The resistors R_1 and R_2 determine the maximum output level $V_Q = R_2/R_1$ URA (URA = 1.25 V); URA can be adjusted with R_1 or R_2, respectively.

The operational amplifiers WA1 and WA2 can be used as required, e.g. as voltage followers after the output holding capacitors (TA1, TA2).

Timing diagram **Clock synchronization pulse**



The transmitting pulses $\overline{SE}_1$, $\overline{SE}_2$ and the receiving pulses $\overline{EE}_1$, $\overline{EE}_2$ can be assigned to any one of the 32 time sequences.

For short distance operation ($\overline{SE}_1 = \overline{SE}_2$ = L), the Codec generates the transmitting and receiving pulses internally. It assigns time sequence 0 to channel 1 and time sequence 16 to channel 2.

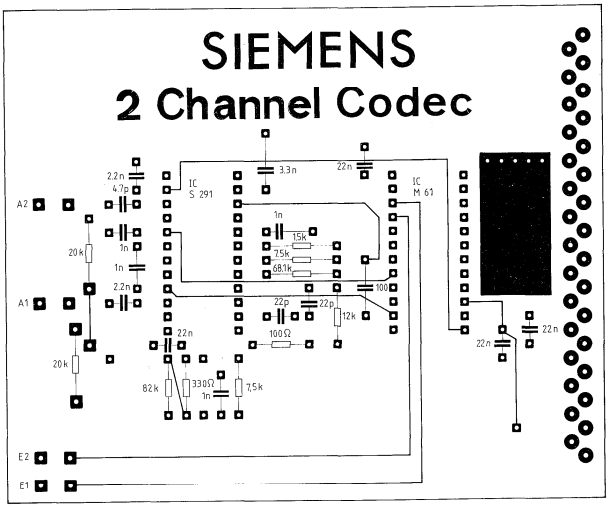
Pin assignments of the evaluation board

1	0 V Analog	11	N.C.	21	+12 V	V_{GG}
2		12	$\overline{SE}_2$	22	N.C.	
3		13	$\overline{SE}_1$	23	N.C.	
4		14	PCM A	24	N.C.	
5	+5 V V_{DD}	15	PCM E	25	N.C.	
6	−5 V V_{SS}	16	$\overline{EE}_2$	26	N.C.	
7	0 V Digital	17	$\overline{EE}_1$	27	−5 V	V_{SS}
8		18	Clock CLK, 2.048 MHz	28	N.C.	
9		19	$\overline{SYE}$	29	+5 V	V_{DD}
10		20	N.C.	30	N.C.	
				31	N.C.	

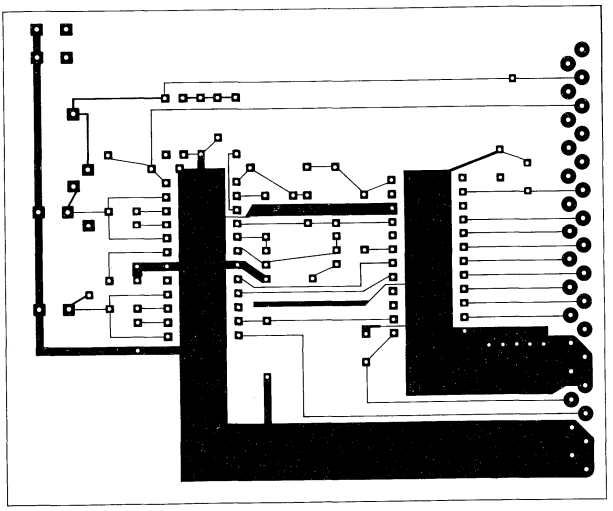
Pins 5 and 29 (+5 V)
6 and 27 (−5 V) must be connected together on the female connector.

Interconnect 0 V analog and 0 V digital with low resistance on the female connector and connect to 0 V of the power supply.

PCB for 2-channel Codec



Front side of PCB



Back of PCB

Decoding:

The 8-bit word received from the PCM 30/32 through the input PCME of the SM 61 A is expanded digitally to a word length of 13 bits and passed to the D/A converter. The sum weighting current at IA is connected to the current-voltage converter of the bipolar circuit, whose output voltage is connected to TAM, the input of the sample and hold section. The resulting analog voltage of the channel is held by the 2.2 nF capacitors at TA_1 and TA_2, respectively, and via the two op amps in S 291 and the external low-pass filters to the analog output channel.

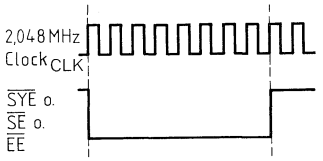
Encoding:

The bandwidths of the analog AF signals from channels 1 and 2 are limited by input low-pass filters and connected alternately via the input sample and hold circuits to the positive inputs of the comparator (see timing diagram). The common 3.3 nF hold capacitor for the two channels is connected to the TEM pin of the sample and hold switches. In order to determine the sign of the sampled value, the PCM word 00000000 is generated in the converter register and transmitted as analog value zero. This ensures that the weighting current IA is 0 and that the voltage at the negative input is also 0, via the current-voltage converter. The comparator thus makes a decision about the sign, and the direction of the reference current from IA_2 (S 291) to IE (SM 61 A) is switched via VA (sign output SM 61 A), connected to VE (sign input S 291). The next bit is now set to 1, and the new 8-bit word is converted to 12 bits, the corresponding weighting current connected to the current-voltage converter, and the voltage proportional to the weighting current compared with the sampled value in the comparator. The comparator decision indicates whether the bit is to be retained (if $V_{Sample} \geqq V_{Weight}$) or reset to zero. This approximation is carried out step by step until the last bit is reached, i.e. until the best possible approximation has been achieved. The final 8-bit word representing the sampled value can now be shifted out via PCMA with a decreasing significance, each second bit being inverted in the process.

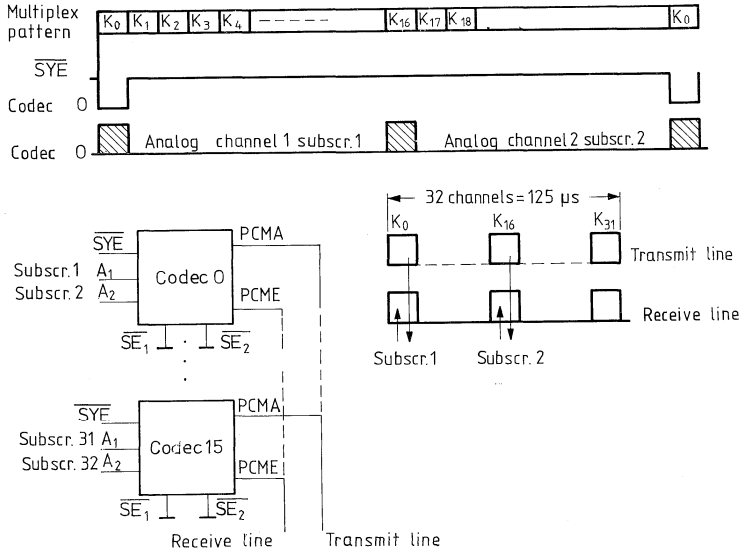
Timing

All control pulses have the width of one word within the channel pattern (≙ 8 bit PCM), synchronized with the pulse edge of the 2.048 MHz clock. The duration of one clock period would basically be sufficient for the synchronizing pulse $\overline{SYE}$, with a synchronous negative-going edge, but the length is not restricted.

Timing diagram

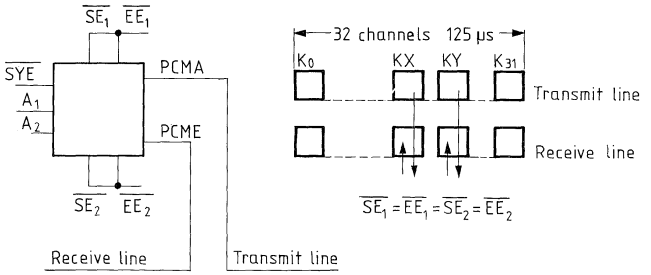


Codec for short distance operation



Decoupling in timing from the multiplex line

In this operating mode, the transmitting and receiving pulses for an analog channel have the same channel position. Basically, the channel position of the synchronization pulse $\overline{SYE}$ may be selected as required.

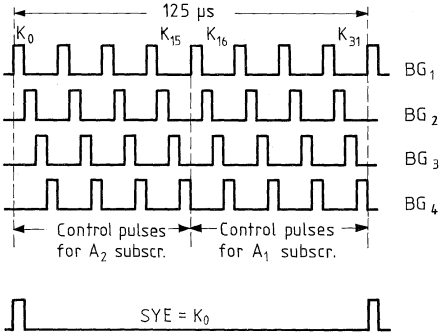


However, difference in the propagation delay of a PCM word will occur, depending on the selected channel position of $\overline{SYE}$. For example, assume that $\overline{SYE} = \overline{SE_1} = \overline{EE_1} = K_0$ in the channel pattern and $\overline{SE_2} = \overline{EE_2} = K_{16}$. A PCM word received from the receive line of the multiplex system at time interval K_0 will then be transferred to the converter register and decoded only after a further 125 µs, with the next synchronization pulse at time interval K_0. The same applies to the PCM word accepted during time interval K_{16} and for the PCM words to be transmitted. If, however, $\overline{SE_1} = \overline{EE_1} = K_0$, $\overline{SE_2} = \overline{EE_2} = K_{16}$ and $\overline{SYE} = K_1$, then the PCM word received during K_0 is transferred to the converter register during interval K_1 and the word received during K_{16} is transferred during interval K_{17}. The same applies to the PCM words to be transmitted. Similar considerations apply to each channel allocation constellation; these lead to

Muldem control for minimum propagation delay

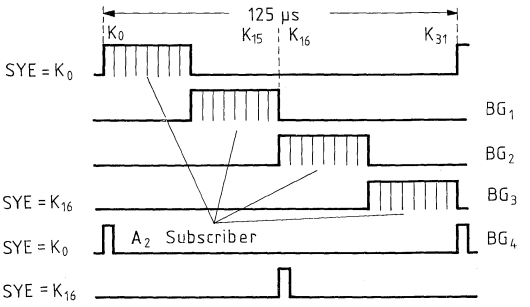
In the case of an arrangement with uniform synchronization pulse $\overline{SYE}$ for all 16 Codecs, for example at channel time K_0, channels K_0 and K_{16} would consequently be specified as Codec transfer channels $\ddot{U}_1 = K_0$ and $\ddot{U}_2 = K_{16}$. A control requirement is the condition that channel $\ddot{U}_1$ is assigned to an A_2 subscriber ($\overline{SE_2} = \overline{EE_2}$) and that channel $\ddot{U}_2$ is assigned to an A_1 subscriber ($\overline{SE_1} = \overline{EE_1}$).

A Muldem PC board BG with n Codecs forms $2n$ channels of the multiplex system. If the BG is controlled such that the $2n$ control pulses ($\overline{SE} = \overline{EE}$) of the BG are distributed uniformly throughout the pattern, then the above condition is fulfilled if the A_2 connections of the Codecs are assigned to Channel 0...15 and the A_1 connections to Channel 16...31 on all BGs (Number $32/2n$).



Subscriber/channel allocation for minimum PCM propagation delay with uniform channel distribution and uniform synchronization pulse

In the case of a block assignment of the mulitplex channels per BG, i.e. immediately adjacent, the distribution of connections for each BG must again start with an A_2 connection (remaining distribution as required), if $\overline{SYE} = K_0$ is also true. This results, with uniform BGs in connection of an A_2 subscriber to channel 16, which means that a second synchronization pulse $\overline{SYE} = K_0$ is required. With two synchronization pulses, the following division seems advisable: Codecs of the first half of the multiplex frame receive $\overline{SYE} = K_0$ and the Codecs for the second half receive $\overline{SYE} = K_{16}$.



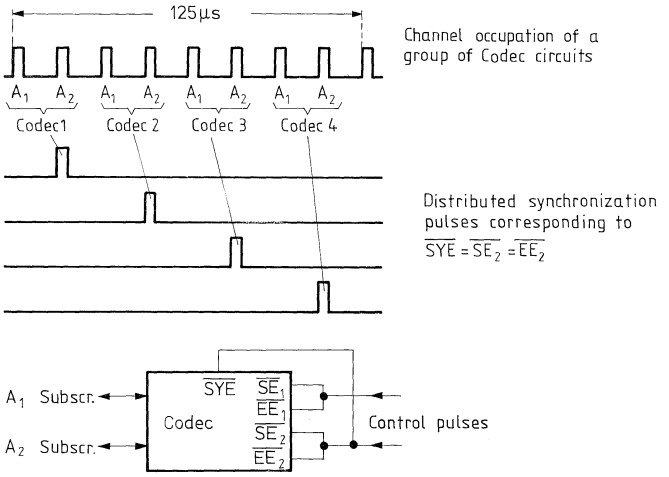
Subscriber/channel allocation for minimum PCM propagation delay with the channels allocated in blocks

A uniform synchronization pulse per BG or Muldem offers the advantage of better control facilities of all synchronously running converters; however, a second synchronization pulse in addition to the control pulses is required and problems may occur with the voltage supply (voltage drops, coupling). An alternative solution would be the distributed synchronization, where the control pulses carry out the synchronization tasks.

The rule is very simple:

$$\overline{SYE} = \overline{SE_2} = \overline{EE_2}$$

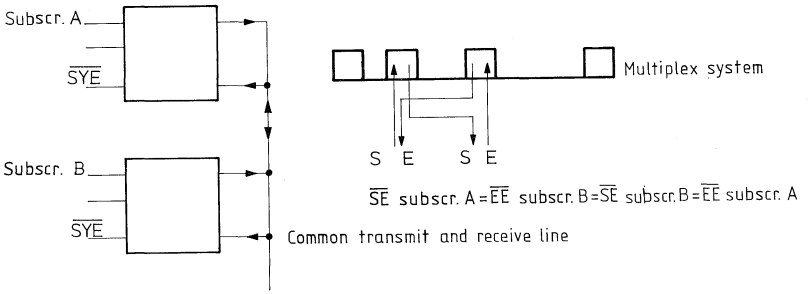
The synchronization pulse is thus identical with the control pulse for the A_2 subscribers and can be connected directly on the chip. The converter timings of all Codecs will then be displaced by 2 channels with respect to each other.



Subscriber/channel allocation for minimum PC propagation display with distributed synchronization

Switching operation

In this operating mode, the transmitting and receiving lines of each multiplex system are identical. In contrast to the operating modes described previously, no coupling matrix is required (physical through connection: transmitting line subscriber X, receiving line subscriber Y; time offset between transmitting channel subscriber X and receiving channel subscriber Y) in order to permit calls between subscribers whose Codecs are connected to the same transmitting and receiving lines.



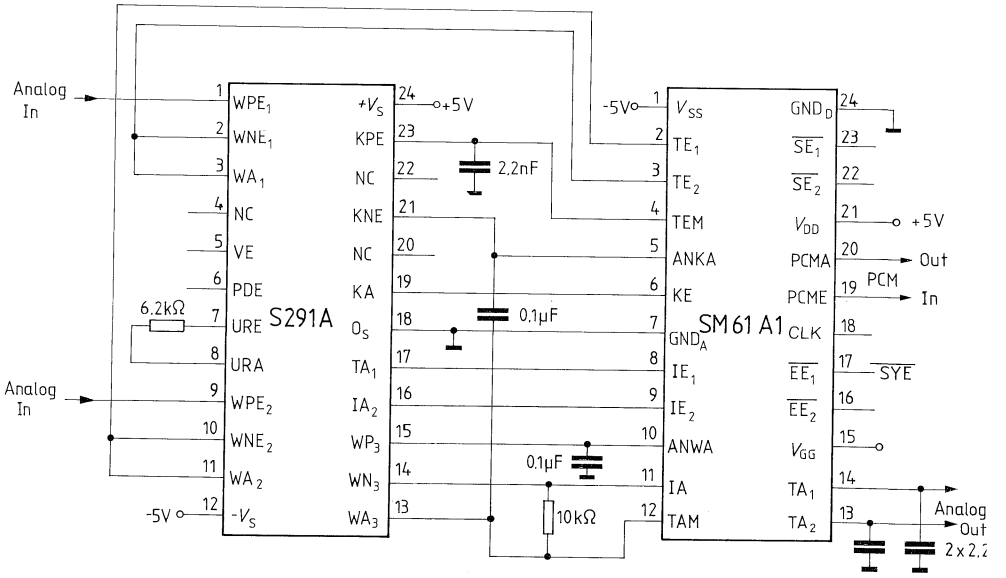
Switching operation

Advanced information

Type	Ordering code	Package outline
SM 61 A1	Q67100–Z134–S1	Figure No. 3
S 291 A	Q67000–A1388–S1	Figure No. 2

In addition to the features of the SM 61 A/S 291, the PCM 2-channel Codec SM 61 A1 (S 291 A) has the following features:

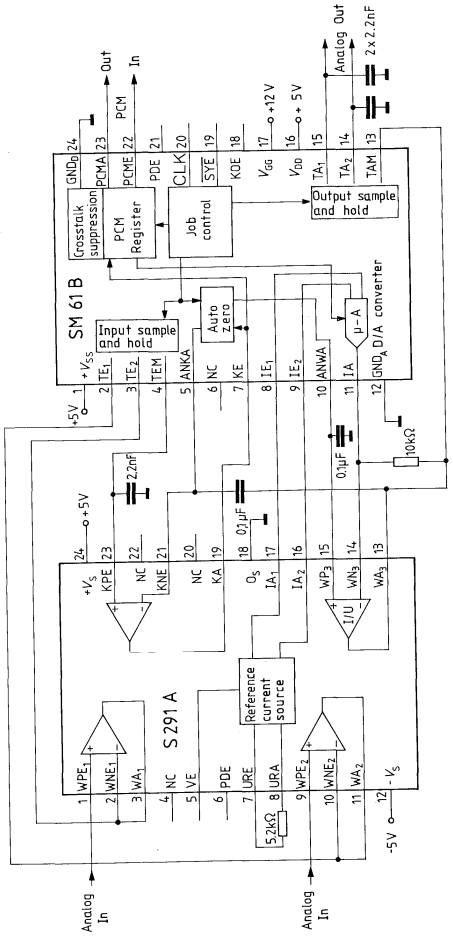
- Power-down mode
- Low power dissipation (75 mW/channel)
- Small number of external components



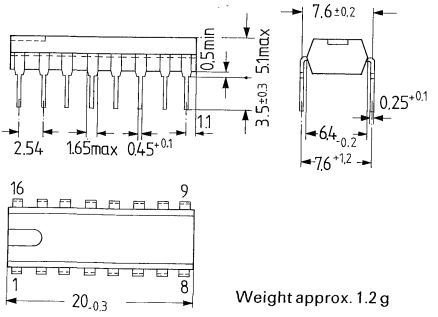
Advanced information

Type	Ordering code	Package outline
SM 61 B	Q67100-Z134-S2	Figure No. 3
S 291 A	Q67000-A1388-S1	Figure No. 2

The PCM 2-channel Codec SM 61 B/S 291 A has, in addition to the features of the SM 61 A1/ S 291 A, a switching facility between A-law and μ-law. The μ-law companding is used mainly in USA and is standardized in accordance with CCITT.



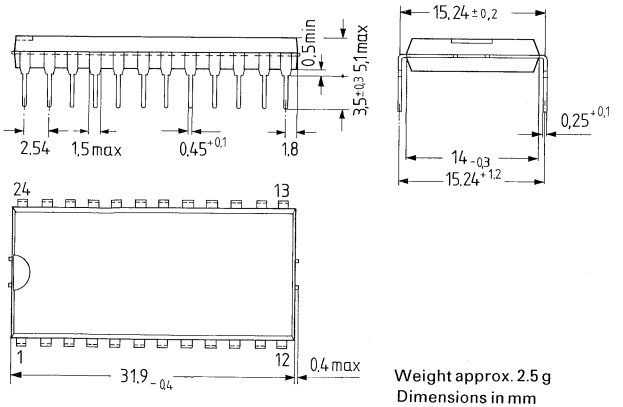
Plastic plug-in package 20 A 16 DIN 41866
16 pins, DIP



Weight approx. 1.2 g

Figure 1

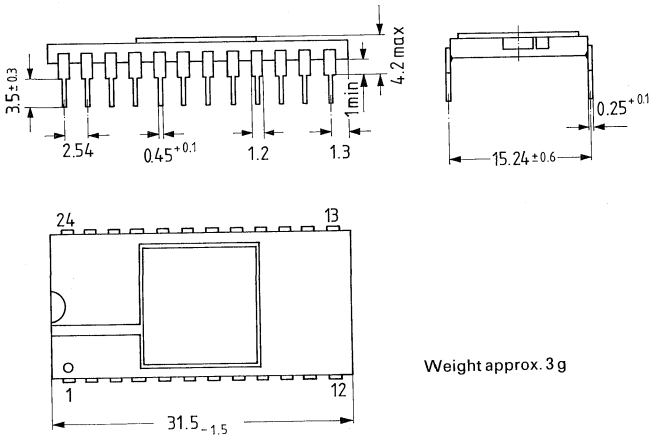
Plastic plug-in package 20 A 24 DIN 41866
24 pins, DIP



Weight approx. 2.5 g
Dimensions in mm

Figure 2

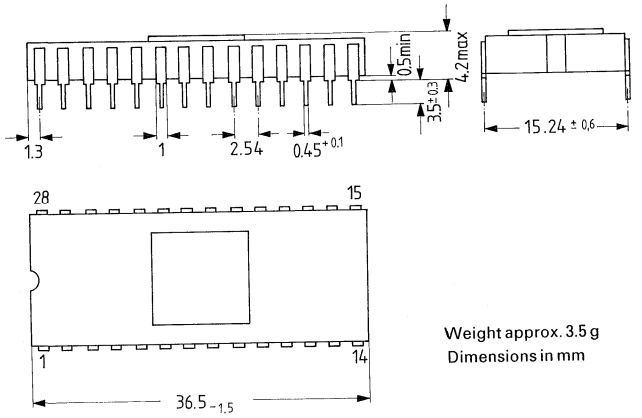
Ceramic package
24 pins, DIC



Weight approx. 3 g

Figure 3

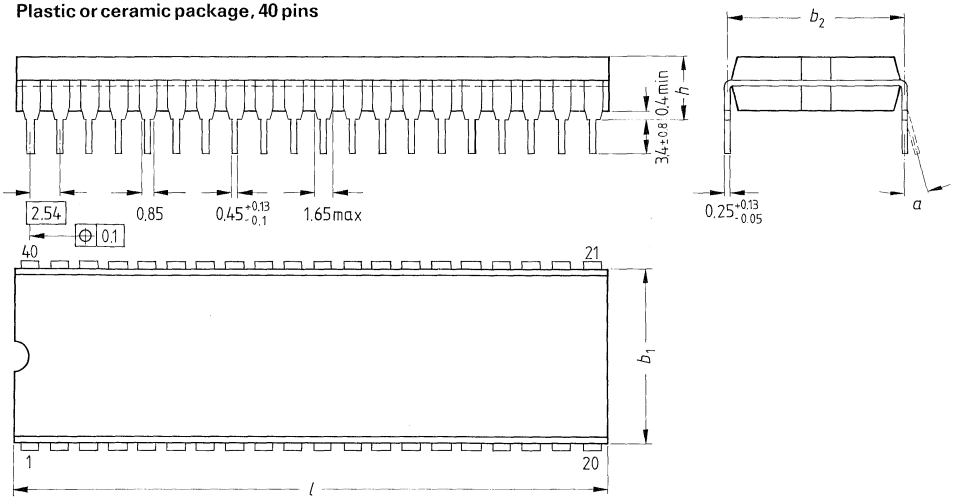
Ceramic package
28 pins, DIC



Weight approx. 3.5 g
Dimensions in mm

Figure 4

Plastic or ceramic package, 40 pins



Version	b_1	b_2	h max.	l	a
Plastic (P)	$14_{-0.6}$	15.24 ± 0.2	5	$52_{-1.5}$	0...15°
Ceramic	15.3_{-1}	15.25 ± 0.5	5	$51.5_{-1.5}$	0°

Figure 5 Dimensions in mm

Memory Devices

Memory Devices

Summary of available microcomputer memory devices

See the Microcomputer Data Book 8080, Edition 1979/80, for detailed data

Type	Organization	Techn.	Operating mode	Supply voltage (Read) V	Access time (max.) ns	Number of pins
RAM circuits (Random Access Memory)						
SAB 2102A-4-	1 024 x 1	NMOS	stat.	+ 5	450	16
SAB 2102A-6-	1 024 x 1	NMOS	stat.	+ 5	650	16
SAB 2102AL-4-	1 024 x 1	NMOS	stat. Low Power	+ 5	450	16
SAB 2104A-1-	4 096 x 1	NMOS	dyn.	± 5; + 12	150	16
SAB 2104A-2-	4 096 x 1	NMOS	dyn.	± 5; + 12	200	16
SAB 2104A-3-	4 096 x 1	NMOS	dyn.	± 5; + 12	250	16
SAB 2104A-4-	4 096 x 1	NMOS	dyn.	± 5; + 12	300	16
SAB 2111A-4-	256 x 4	NMOS	stat.	+ 5;	450	18
SAB 2114-	1 024 x 4	NMOS	stat.	+ 5	450	18
SAB 2114-2-	1 024 x 4	NMOS	stat.	+ 5	200	18
SAB 2114-3-	1 024 x 4	NMOS	stat.	+ 5	300	18
SAB 2114L-	1 024 x 4	NMOS	stat. Low Power	+ 5	450	18
SAB 2114L-3-	1 024 x 4	NMOS	stat. Low Power	+ 5	300	18
SAB 2117-2-	16 384 x 1	NMOS	dyn.	± 5; + 12	150	16
SAB 2117-3-	16 384 x 1	NMOS	dyn.	± 5; + 12	200	16
SAB 2117-4-	16 384 x 1	NMOS	dyn.	± 5; + 12	250	16
SAB 2142-	1 024 x 4	NMOS	stat.	+ 5	450	20
SAB 2142-2-	1 024 x 4	NMOS	stat.	+ 5	200	20
SAB 2142-3-	1 024 x 4	NMOS	stat.	+ 5	300	20
SAB 2142L-3-	1 024 x 4	NMOS	stat. Low Power	+ 5	300	20
SAB 2147-	4 096 x 1	NMOS	stat.	+ 5	70	18
SAB 2147-3-	4 096 x 1	NMOS	stat.	+ 5	55	18
SAB 5101L-	256 x 4	CMOS	stat. Low Power	+ 5	650	22
SAB 5101L-1-	256 x 4	CMOS	stat. Low Power	+ 5	450	22
SAB 8102A-4-	1 024 x 1	NMOS	stat.	+ 5	450	16
SAB 8111A-4-	256 x 4	NMOS	stat.	+ 5	450	18
ROM circuits (Read Only Memory)						
SAB 8308-	1 024 x 8	NMOS	stat.	± 5; + 12	450	24
SAB 8316A-	2 048 x 8	NMOS	stat.	+ 5	450	24
EPROM circuits (Electrically Programmable ROM)						
SAB 1702A-	256 x 8	PMOS	stat.	+ 5; - 9	1000	24
SAB 1702A-2-	256 x 8	PMOS	stat.	+ 5; - 9	650	24
SAB 1702AL-2-	256 x 8	PMOS	stat. Low Power	+ 5; - 9	650	24
SAB 2704-	512 x 8	NMOS	stat.	± 5; + 12	450	24
SAB 2708-	1 024 x 8	NMOS	stat.	± 5; + 12	450	24
SAB 2708-1-	1 024 x 8	NMOS	stat.	± 5; + 12	350	24
SAB 2716-	2 048 x 8	NMOS	stat.	+ 5	450	24
SAB 2716-1-	2 048 x 8	NMOS	stat.	+ 5	350	24
SAB 2716-2-	2 048 x 8	NMOS	stat.	+ 5	390	24
SAB 2732-	4 096 x 8	NMOS	stat.	+ 5	450	24
SAB 2758-	1 024 x 8	NMOS	stat.	+ 5	450	24
SAB 4702A-	256 x 8	PMOS	stat.	+ 5; - 10	1700	24
SAB 8702A-	256 x 8	PMOS	stat.	+ 5; - 9	1000	24
SAB 8708-	1 024 x 8	NMOS	stat.	± 5; + 12	450	24

Technical information

Since the announcement of the first highly integrated semiconductor memory devices in 1969, this type of ICs has developed rapidly. The advantages of manufacturing memories in semiconductor technology are:

- Low physical volume due to high memory density
- Low power consumption
- High operating speed
- High reliability
- Uniform construction technology for memory and logic circuits
- High flexibility with respect to memory capacity and type of organization in the development of memory systems
- Falling costs per unit of information

These advantages are fully utilized by the large advances in semiconductor technology and circuit techniques.

Memory types

The following are the types of semiconductor memories which are widely used.

The most widely used type of memory is the *random access memory (RAM).* These are memory circuits where the memory elements are arranged in form of a matrix and are selected by using row and column lines as coordinates. Depending on the application, they are organized in words or single bits. Their applications range from memories in small control systems to main memories in the central processing units of large computer systems.

In the case of *read only memories (ROM),* the contents of the memory are written in either mechanically or electronically during manufacture. Again, the memory cells are arranged in the form of a matrix and can be read separately. Their applications range from storage of table values for mathematical functions via storage of microprograms and functional sequences up to use as code converters, character generators, etc.

Electrically reprogrammable read only memories are programmed and, if necessary, erased by the user himself. Their type of organization and their possible applications are similar to those of mask programmed read only memories.

In the case of optically erasable *EPROMs (erasable and programmable ROMs),* the contents of the memory can be cleared completely by exposing the device to ultraviolet light. Reprogramming is then carried out by application of suitable electrical pulses. The stored information remains in the memory even when the supply voltage is switched off.

The *electrically erasable and programmable ROM (EEPROM)* offers the further advantage that the complete contents of the memory can be erased by an electric pulse. Reprogramming is carried out in the same manner as for the EPROM.

Characteristic parameters of memories

The specific characteristic parameters of memories defined below are used for comparison of semiconductor memory circuits.

Memory capacity: Number of memory cells in a memory device. This is specified, depending on the organization in words × bits (word length) or bits, 1 KBit corresponding to 1024 bits.

Access time: The maximum time from addressing of a memory element until the information is available at the data output of the memory device.

Cycle time: The minimum time between two sequential write or read operations. In the case of random access memories, the time indications are normally specified for two different operating modes, namely either pure write or read cycles or *read-modify-write (RMW)* cycles, where the contents of a memory cell are read and then new information is returned to the same memory cell within one cycle. As it is possible to read information from semiconductor memory circuits without destroying it *(NDRO = non-destructive read out),* which means that the information does not need to be written back into the memory after reading, the cycle time is not much longer than – and in the best case – even to the access time.

Power dissipation: The electrical power dissipation is specified as a total power dissipation or power dissipation per bit. It is also possible to define the current consumption for the standby mode and the operating mode.

Electrical operating conditions: These contain details on the number and values of the supply voltages, levels of input voltages, current and voltage waveforms at the data output.

Operating temperature range: The temperature range within which the memory operates reliably within its electrical specification.

Memory principles

Volatile memories

Static RAM

In the case of static memories, the memory elements are formed by two inverters with a feedback circuit (bistable flipflop), the logical information "0" and "1" being assigned to the two stable states. In the basic circuit in figure 1, the two load resistors are replaced by two transistors T_3 and T_4 with a fixed bias voltage due to the reduced space requirements for transistors.

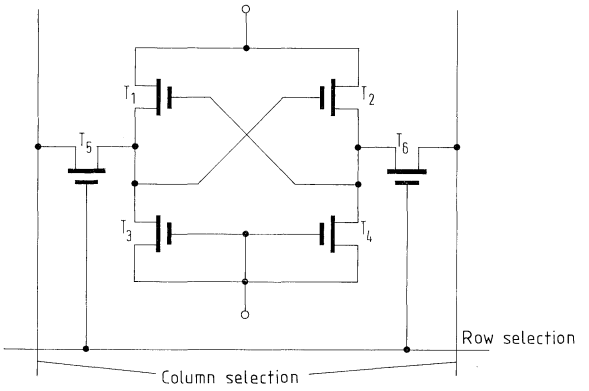


Figure 1

The transistors T_5 and T_6 are used for selection of the memory cells. If these transistors are made to conduct by the row selection line, then the information can be detected during reading by means of the potential difference between the column lines, while the flipflop is set to the required state via these lines during writing. The stored information remains stored as long as the supply voltage remains within its specified range. As a current continuously flows through one of the two halves of the flipflop, the power requirements of static semiconductor memories are higher than those of dynamic memories (see next section).

Dynamic RAM

In dynamic memory elements, the information is stored as a charge in a capacitance. The basic circuit shown in figure 2 represents a so-called one-transistor cell in which the information appears as a potential jump on the data line, depending on the capacitor charge, as soon as

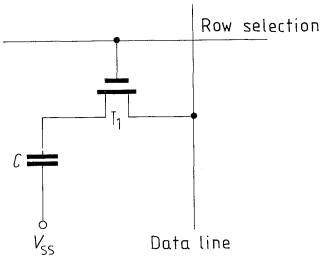


Figure 2

transistor T_1 is caused to conduct via the row selection line. Due to the unavoidable leakage currents, the information (capacitor charge) must be refreshed periodically. Refreshing is carried out in the circuit by read cycles at the refresh addresses, the whole row being regenerated by selection of a memory element. As the leakage of the capacitor charge is accelerated at higher temperatures, the minimum refresh time (normal value: 2 ms) requires particular attention at the maximum permissible operating temperature. Due to the few components required, large memory capacities can be implemented per device.

Non-volatile memories

ROM

The contents of mask programmed ROMs are loaded by the manufacturer in accordance with the customer's specifications. Wherever programming of a memory cell is required within a matrix arrangement of rows and columns, an MOS transistor is generated during the manufacturing process of the device. Correspondingly, cells which are not programmed are represented by absence of such transistors.

In a matrix arrangement as shown in figure 3, the row selection line is connected to the gates of all memory transistors in a row.

The drain terminals of all memory transistors in one column are connected to one data line.

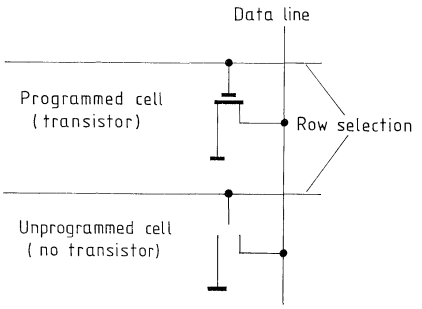


Figure 3: Cell selection in an ROM

A cell is selected by applying a logical "1" potential to a row selection line, in accordance with the required cell address, and applying logical "0" potential to all other row selection lines. If the cell is an MOS transistor, then it conducts and pulls the data line down to logical "0" potential. If the cell is not programmed, no current flows and the data line remains at the logical "1" potential. The data line signal is amplified and connected to a data output terminal.

The simple construction of such a memory matrix permits implementation of large memory densities and thus high memory capacities per device.

EPROM, EEPROM

The memory element of the electrically reprogrammable ROM is the SIMOS transistor (*S*tacked Gate *I*njection *MOS*). It contains a lower, floating gate and an upper control gate, as shown in figure 4. The floating gate is used as a charge storage element: The cell is programmed by injection of high energy electrons into the floating gate. The charge cannot be dissipated as the floating gate is completely isolated from its surroundings.

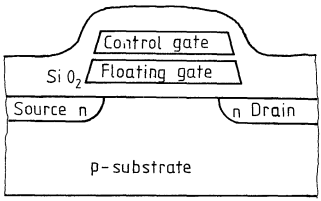


Figure 4: SIMOS transistor

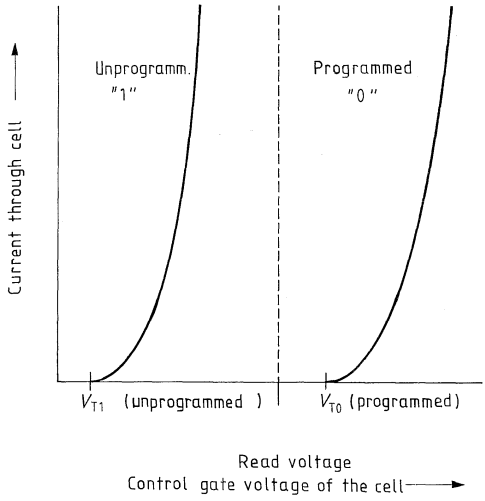


Figure 5: Threshold voltage shift of the cell

Charging of the floating gate causes the threshold voltage of the cell to be shifted. As shown in figure 5, the threshold voltage originally has a very low value, which means that selection of the cell by means of a voltage at the control gate causes a current to flow through the memory transistor. Programming shifts the threshold voltage to such a high value that the read voltage at the control gate can no longer switch the cell to the conducting state.

In a matrix arrangement similar to that of an ROM, the status of the selected cell (programmed = 0, unprogrammed = 1) is detected by evaluating the current flowing through the cell after connection of the read voltage. A current flows from drain to source of the cell only if the cell is not programmed; a programmed cell remains cut off.

The stored charge of a cell is changed only during programming and erasing. Storage without voltage or read operations do not influence the programmed state of the cell. For this reason, EPROMs and EEPROMs can be used just like ROMs.

In the case of the optically erasable EPROM, the contents are erased by exposing to ultraviolet light. The photo effect then permits the electrons stored in the floating gate to flow through the oxide to the substrate.

In the case of the electrically erasable EEPROM, the memory cell is additionally equipped with an erase area, in which the floating gate is separated from an erase electrode by a particularly thin layer of oxide. If a high voltage is applied to this electrode, then the electrons on the floating gate "tunnel" through the thin oxide layer to the erase electrode, due to the high field strength. This operation is considerably faster than optical erasure.

Memory technologies

Semiconductor memories are divided into two groupes, based on the manufacturing methods used.

Bipolar memories

Bipolar memory circuits consist of transistors in TTL (*T*ransistor-*T*ransistor *L*ogic) or ECL (*E*mitter *C*oupled *L*ogic) technology, the ECL circuit being characterized by particularly high speeds. Due to their compatibility with the corresponding circuit technology, they are very easy to use. On the other hand, they have a high power consumption and a low integration density. Their use is advantageous wherever a high operating speed is required.

MOS memories (MOS = *M*etal *O*xide *S*emiconductor)

In the case of MOS memory circuits, MOS field effect transistors in P or N channel technology are used. Circuits in N channel technology can be integrated to a higher degree, have a relatively high operating speed due to the greater mobility of the charge carriers, and are compatible with TTL technology. In general, MOS technology offers all prerequisites for low cost manufacture of memory circuits with large capacities, due to the simplicity of the structures, the small number of manufacturing steps, and the electrical characteristics of MOS transistors.

Testing techniques

The correct function of semiconductor memory devices can be affected by a large number of technological and circuit error mechanisms. It is thus not sufficient to check the circuits for addressability and for the ability to store the logical information "0" and "1". Memory circuits have a tendency to react critically to specific addressing sequences combined with write/read operations (pattern sensitivity). For this purpose, a test unit with which the required write/read cycles with non-linear addressing (test pattern) can be generated. In addition, experience has shown that the testing effort and costs increase as the square of the number of bits. These high testing requirements make it necessary to use complex computer controlled systems with programmable test pattern generators and adjustable timing voltage conditions, with which all critical operating states can be simulated.

In order to guarantee the high reliability of semiconductor memory devices, they are subjected to so-called preaging, where the devices are operated under increased voltage and temperature conditions ("Burn in") in order to discover any weak points, which could cause early failures during normal use.

Special handling of MOS memory devices

Although MOS circuits are protected to a great degree against destruction by static charges by suitable integrated protective structures, a few rules must be observed when handling such circuits.

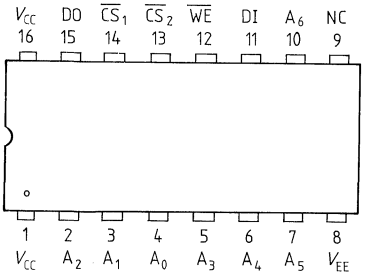
- MOS devices should always be stored in suitable packing materials (conductive foam, short-circuit brackets) and should be placed only on conducting surfaces.
- All benches, equipment, and test jigs must be grounded.
- Persons who work with MOS circuits should be connected to ground (neutral conductor) via a resistor of at least 100 kΩ.
- It is not permissible to handle MOS components with their pins.

Preliminary data

Type	Ordering code	Package outline
GXB 10147 A	Q67000-S38	Figure No. 1

- Very high speed ECL memory
- Access time typ. 10 ns
- Fully decoded
- 128 × 1 bit organization
- Memory expansion by chip enable inputs (chip select)
- OR-tie capability
- Static mode of operation, no refresh necessary
- Stabilized characteristic of the current consumption
- Negative *TC* of current consumption, self stabilizing
- 16 pin metal ceramic package
- Compatible with Motorola MCM 10147 AL, Fairchild F 10405
- Compatible with logic families ECL 10 k and Fairchild 95 k

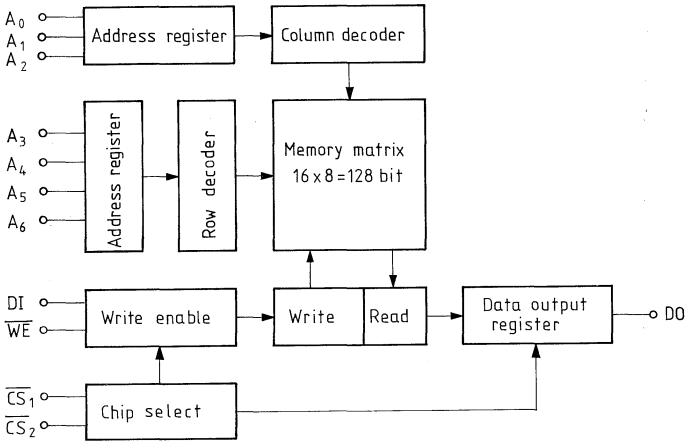
Pin configuration (top view)



Pin names

A_0–A_6	Address inputs
DI	Data input
$\overline{CS}_1$, $\overline{CS}_2$	Chip select
$\overline{WE}$	Write enable (read/write)
DO	Data output
V_{EE}	Supply voltage (–5.2 V)
V_{CC}	Ground
NC	Not connected

Block diagram



Absolute maximum ratings[1])

Supply voltage	V_{EE}	–7	V
Input voltages	V_I	0 to V_{EE}	V
Output current	I_O	50	mA
Ambient temperature	T_{amb}	0 to 85	°C
Storage temperature	T_s	–55 to 125	°C

[1]) Stresses above those listed unter "Absolute maximum ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC characteristics

$T_{amb} = 25°C$, $V_{EE} = -5.2\,V \pm 10\,\%$, $R_L = 50\,\Omega$ with respect to $-2.0\,V$
Fan cooling with 500 fpm linear

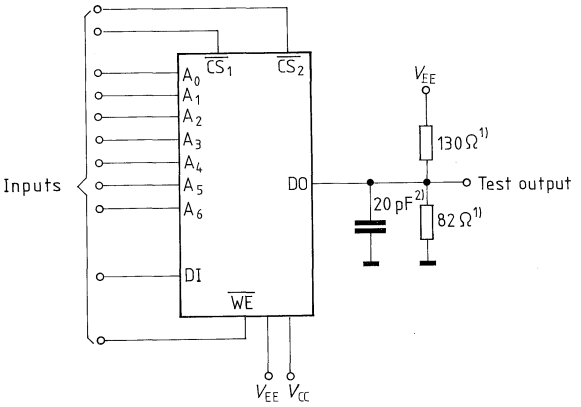
		Test conditions	Min.	Typ.	Max.	Unit
H-input voltage	V_{IH}		−1.105		−0.810	V
L-input voltage	V_{IL}		−1.850		−1.475	V
H-output voltage	V_{OH}	$R_L = 50\,\Omega$ to $-2.0\,V$	−0.960		−0.810	V
L-output voltage	V_{OL}	$V_{IL\,min}$ at A, DI, $V_{IH\,min}$ at $\overline{WE}$, $V_{IL\,max}$ at $\overline{CS_1}$, $\overline{CS_2}$	−1.900		−1.650	V
H-input current A, DI, $\overline{CS}$	I_{IH}				35	µA
H-input current $\overline{WE}$	I_{IH}				75	µA
L-input current	I_{IL}		−6			µA
Supply current	I_{EE}			80	100	µA

AC characteristics

$V_{EE} = -5.2\,V \pm 10\,\%$

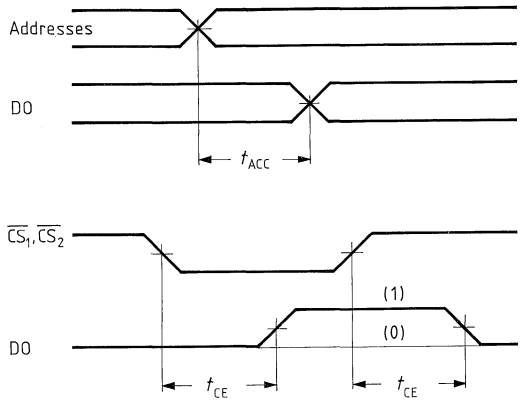
		25°C			85°C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Access time	t_{ACC}		10	12			14	ns
Enable time	t_{CE}		6.5	8			9	ns
Write pulse width	t_{WW}	8			8			ns
Write recovery time	t_{WR}			8				ns
Set-up time A to $\overline{WE}$	t_{AWS}	4						ns
Set-up time $\overline{CS}$ to $\overline{WE}$	t_{CWS}	1						ns
Set-up time DI to $\overline{WE}$	t_{IWS}	1						ns
Hold time $\overline{WE}$ to A	t_{WAH}	3						ns
Hold time $\overline{WE}$ to $\overline{CS}$	t_{WCH}	1						ns
Hold time $\overline{WE}$ to DI	t_{WIH}	1						ns

Access time test circuit



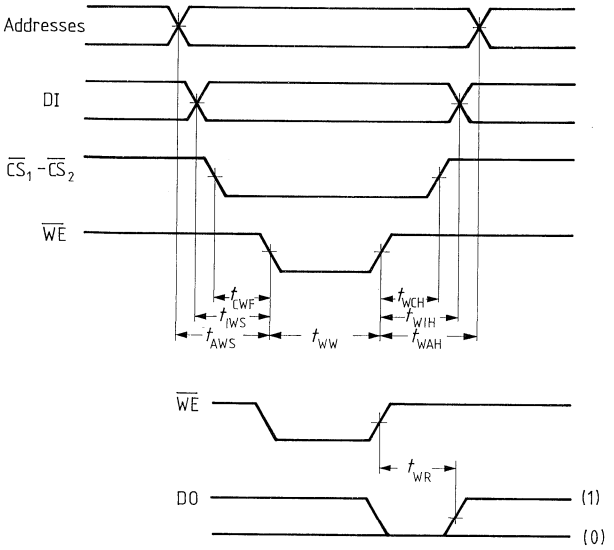
[1]) The load resistance shall be 50 Ω to –2 V. This test circuit meets the requirement, working with V_{EE}. Other voltage dividers can be used, as long as the general condition is observed.
[2]) Total load capacity, measurement set-up and measuring apparatus included.

Timing diagrams[3])
Read cycle



[3]) Timing points are 50 % of the logical amplitude.

Write cycle


Addresses
DI
$\overline{CS_1}$ - $\overline{CS_2}$
$\overline{WE}$
t_{CWF}
t_{IWS}
t_{AWS}
t_{WW}
t_{WCH}
t_{WIH}
t_{WAH}
$\overline{WE}$
t_{WR}
DO
(1)
(0)

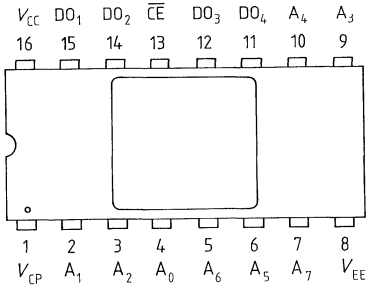
Preliminary data

Type	Ordering code	Package outline
GXB 10149	Q67000–R117	Figure No. 1

The elements are Ni-Cr resistors which can be fused by defined current pulses. The original information L (V_L = –1.65 V to –1.85 V) in the unprogrammed state changes by the programming operation irreversibly to H state (V_H = –0.81 to –0.96 V) in the selected memory locations. Additional 32 test bits are provided for static, dynamic and programming tests.

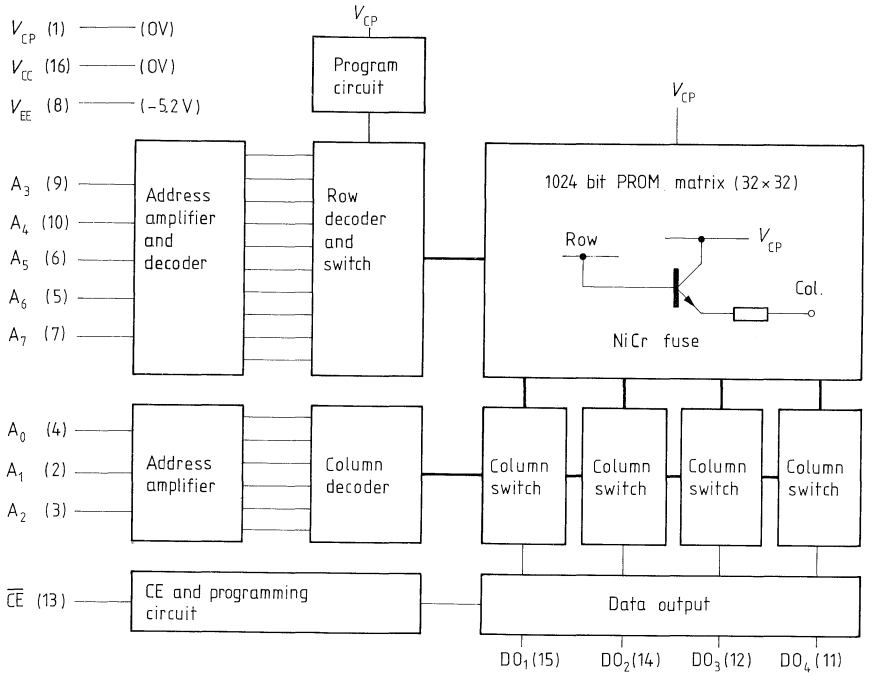
- 256 × 4 bit organization
- Fast access time 12 ns typically
- Fully decoded
- Ceramic package DIC 16
- Compatible with ECL 10 k logic family

Pin configuration
(top view)



A_0 to A_7	Address inputs
$\overline{CE}$	Chip enable
DO_1 to DO_4	Data outputs
V_{EE}	Supply voltage –5.2 V
V_{CP}	Programming voltage
V_{CC}	Ground

Block diagram



Absolute maximum ratings[1])

Read mode ($V_{CP} = V_{CC} = 0\,V$)

Supply voltage	V_{EE}	–7	V
Input voltages	V_I	0 to V_{EE}	V
Output current	I_O	50	mA
Ambient temperature	T_{amb}	0 to 85	°C
Storage temperature	T_s	–55 to 125	°C

Programming mode ($V_{EE} = -5.2\,V \pm 5\%$)

Programming voltage	V_{CP}	7	V
Data out voltage	V_{DO}	4.5	V
$\overline{CE}$ voltage	V_{CE}	–5.6	V
Programming current	I_{CE}	–50	mA

[1]) Stresses above those listed unter "Absolute maximum ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.

DC characteristics

$T_{amb} = 25°C \pm 3°C$, $V_{EE} = -5.2\,V \pm 5\%$, fan cooling min. 500 fpm linear,
$R_L = 50\,\Omega \pm 1\%$ to $2\,V \pm 5\%$

		Test conditions	Min.	Typ.	Max.	Unit
H-input voltage	V_{IH}		−1.105		−0.81	V
L-input voltage	V_{IL}		−1.85		−1.475	V
H-input current	I_{IH}	$V_{IH} = -0.81\,V$			250	µA
L-input current	I_{IL}	$V_{IL} = -1.85\,V$ at all inputs	10			µA
H-output voltage	V_{QH}		−0.96		−0.81	V
L-output voltage	V_{QL}		−1.9		−1.65	V
Supply current	I_{EE}			110		µA

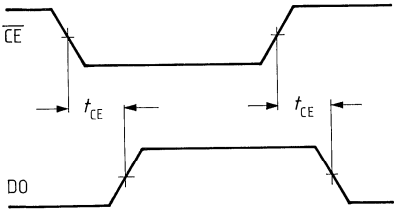
AC characteristics

$T_{amb} = 0°C$ to $85°C$, $V_{EE} = -5.2\,V \pm 5\%$

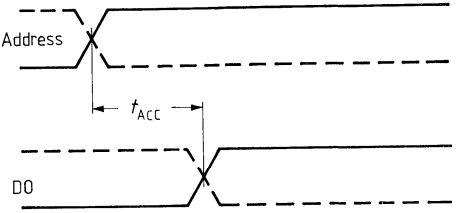
Enable time $\overline{CE}$ to DO	t_{CE}			6		ns
Access time address to DO	t_{ACC}			12		ns

Timing diagrams

Chip enable access time



Address access time



Reference voltage for input and data output signals is −1.29 V

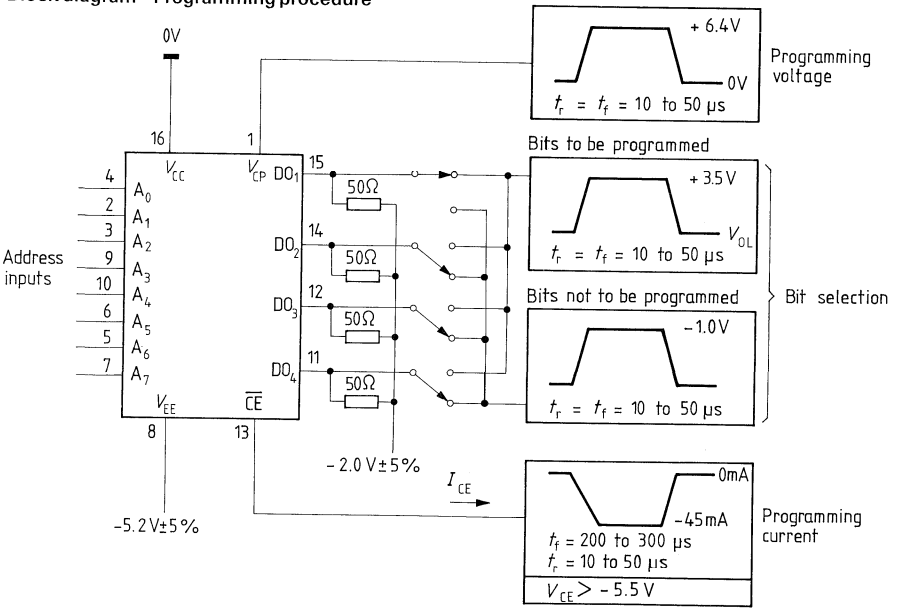
Programming specifications

$T_{amb} = +25°C$, $V_{EE} = -5.2\,V \pm 5\%$

Recommended programming conditions

		Conditions	Limits	Unit
Supply voltage	V_{CC}		0	V
Programming voltage	V_{CP}		$+6.4 \pm 0.1$	V
Bit voltage (selected)	V_{DOS}	Bit to be programmed	$+3.5 \pm 0.2$	V
Bit voltage (not selected)	V_{DOU}	Bit not to be programmed	-1 ± 0.2	V
Programming current	I_{CE}	$V_{CE} > -5.5\,V$	-45 ± 1	mA
Address input voltage	V_{IH}		−0.96 to 0.81	V
	V_{IL}		−1.85 to 1.65	V

Block diagram – Programming procedure



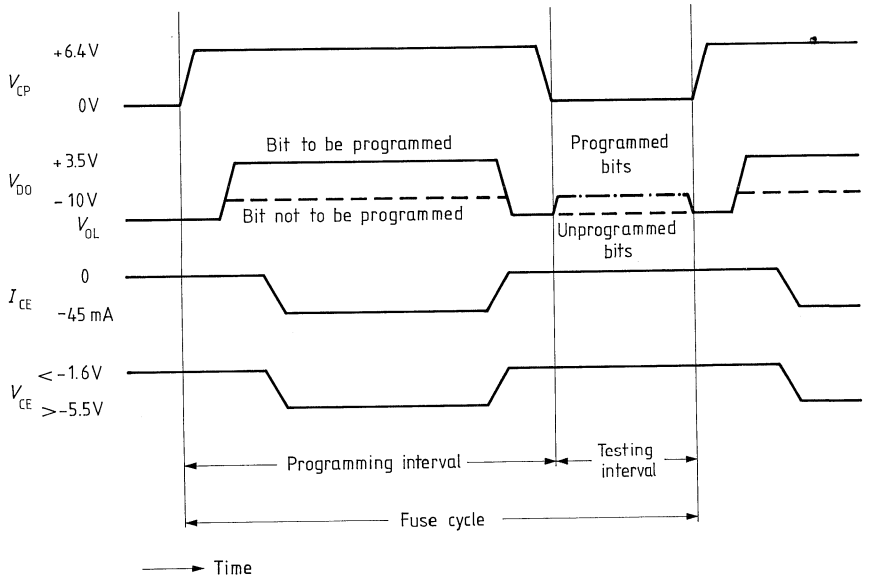
1. Word selection Via addresses A_0 to A_7.

2. Programming operation: Apply programming voltage, bit selection and programming current in this sequence.
Duration of programming current: 2 to 3 ms.
Remove programming current, bit selection and programming voltage in this sequence (see pulse diagram).

3. Read check: V_{CP} at 0 V.
All outputs over 50 Ω at −2 V, V_{CE} at L.
A programmed bit has $V_{QH} \geqq -0.98$ V.
An unprogrammed bit has $V_{QL} \leqq -1.65$ V.

4. Programming time: Typically one programming cycle with 1 ms programming time is sufficient.

Timing diagram



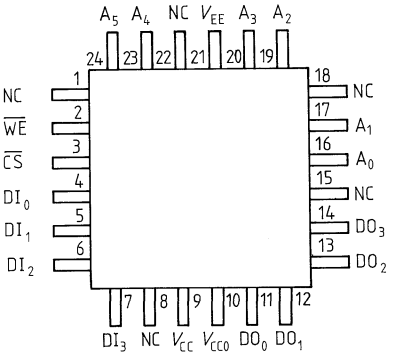
Preliminary data

Type	Ordering code	Package outline
GXB 100 473	Q67000–Q215	Figure No. 4

The GXB 100 473 is a static, high speed random access memory in OXIS technology and is compatible with the ECL 100 k family.

- 64 × 4 bit organization
- Max. access time: 8 ns
- Power dissipation 2.7 mW/bit
- Input and output levels and supply voltage compatible with ECL 100 k family
- Input for chip select
- OR-tie capability

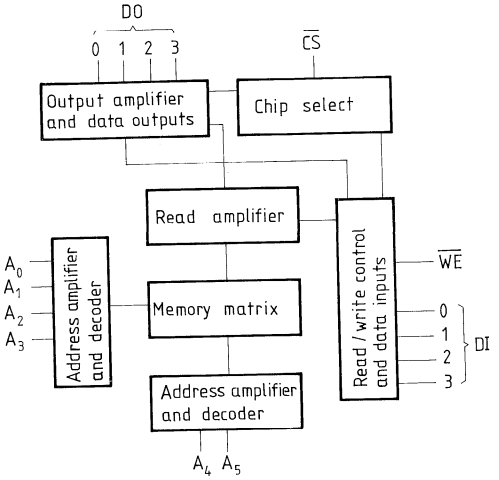
Pin configuration (top view)



Pin names

A_0–A_5	Address inputs
DI_0–DI_3	Data inputs
DO_0–DO_3	Data outputs
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}, V_{CCO}	GND 1, GND 2
V_{EE}	Supply voltage
NC	Not connected

Block diagram



Absolute maximum ratings[1])

Supply voltage	V_{EE}	–4.05 to –4.95	V
Input voltage	V_I	GND to V_{EE}	
Output current	I_O	–50	mA
Ambient temperature	T_{amb}	0 to 85	°C
Storage temperature	T_s	–55 to 125	°C

Functional description

Four of the 256 cells of the memory matrix are selected with the six address inputs A_0 to A_5 via the X and Y decoders.

These four cells can be read or written with new information, depending on the state of the write/read control and the signal at the $\overline{WE}$ input.

During the read cycle, the information from the selected cells is moved via the output amplifier to the data output. The values available at the data input DI have no effect.

During the write cycle, the values available at DI are transferred to the four selected cells. In this mode, the output amplifier is disabled and DO always has "Low" level.

The write/read control and the output amplifier can be disabled or enabled simultaneously via the chip select input $\overline{CS}$. If they are disabled, it is not possible to read from or write into the memory, regardless of the logical values at the remaining inputs. The contents of the memory remain unaffected.

The device is a non-inverting memory, i. e. the logical value written in at DI is identical with the logical value read out at DO. In all operating states, a "Low" level is present at the output, except when a "High" level is read. This characteristic makes it possible to connect the outputs of several devices together, the common output then having "High" level only when a "High" level is generated by a selected chip. With these connections (OR-tied connections), it is possible to assemble virtually unlimited memory capacities.

[1]) Stresses above those listed under "Absolute maximum ratings" may cause permanent damage to the device. Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is, therefore, advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Truth table

Input			Output	Operating mode
$\overline{CS}$	$\overline{WE}$	DI	Open emitter	
H	X	X	L	Disabled
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	H/L	Read "1"/"0"

Operating and test conditions

$T_{amb} = 25°C$, $V_{CC} = 0\,V$, $V_{EE} = -4.5\,V \pm 10\%$, output load $50\,\Omega$ to $-2\,V$

DC characteristics ($T_{amb} = 25°C$)

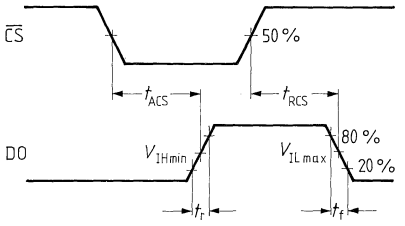
		Test conditions	Min.	Typ.	Max.	Unit
Supply current from V_{EE}	I_{EE}			150		mA
H-output voltage	V_{QH}	$V_I = V_{IH\,max}$	−1025	−955	−880	mV
L-output voltage	V_{QL}	or $V_{IL\,min}$	−1810	−1705	−1620	mV
H-output voltage	V_{QHC}	$V_I = V_{IH\,min}$	−1035			mV
L-output voltage	V_{QLC}	or $V_{IL\,max}$			−1610	mV
H-input voltage	V_{IH}		−1215		−880	mV
L-input voltage	V_{IL}		−1810		−1425	mV
H-input current (A_0–A_5, $\overline{WE}$)	I_{IH}	$V_I = V_{IH\,max}$		15		µA
H-input current ($\overline{CS}$, DI)	I_{IH}	$V_I = V_{IH\,max}$		30		µA
L-input current (A_0–A_5, $\overline{WE}$, $\overline{CS}$, DI)	I_{IL}	$V_I = V_{IL\,max}$		0		µA
Power dissipation	P_{tot}			0.7		W

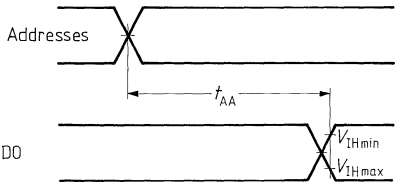
Operating and test conditions

$T_{amb} = 0$ to $85°C$, $V_{CC} = 0\,V$, $V_{EE} = -4.5\,V \pm 10\,\%$

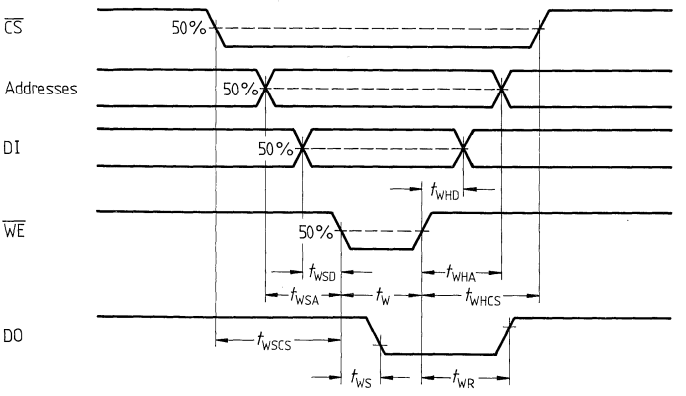
AC conditions

Read cycle		Min.	Typ.	Max.	Unit
Chip select access time	t_{ACS}		5	6	ns
Chip select recovery time	t_{RCS}		5	6	ns
Address access time	t_{AA}		6	8	ns
Rise time	t_r	0.5	0.7	0.9	ns
Fall time	t_f	0.5	0.7	0.9	ns





Write cycle		Min.	Typ.	Max.	Unit
Write pulse width	t_W	8	6		ns
Data set-up time	t_{WSD}	1	0		ns
Data hold time	t_{WHD}	3	2		ns
Address set-up time	t_{WSA}	3	2		ns
Address hold time	t_{WHA}	3	2		ns
Chip select set-up time	t_{WSCS}	1	0		ns
Chip select hold time	t_{WHCS}	2	1		ns
Write disable time	t_{WS}	5	4		ns
Write recovery time	t_{WR}	7	5		ns



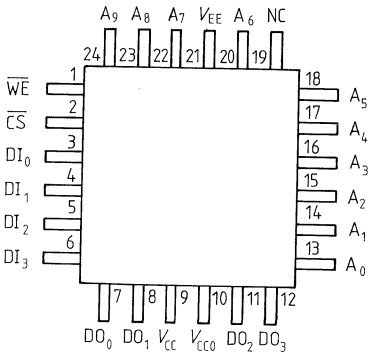
Preliminary data

Type	Ordering code	Package outline
GXB 100 474	Q67000–Q214	Figure No. 4

The GXB 100 474 is a high speed random access memory in OXIS technology and is compatible with the ECL 100 k family.

- 1024 × 4 bit organization
- Max. access time: 25 ns
- Power dissipation: 92 mW/bit
- Input and output levels and supply voltage compatible with ECL 100 k family
- Input for chip selection
- OR-tie capability
- Pin compatible with Fairchild F 100 474

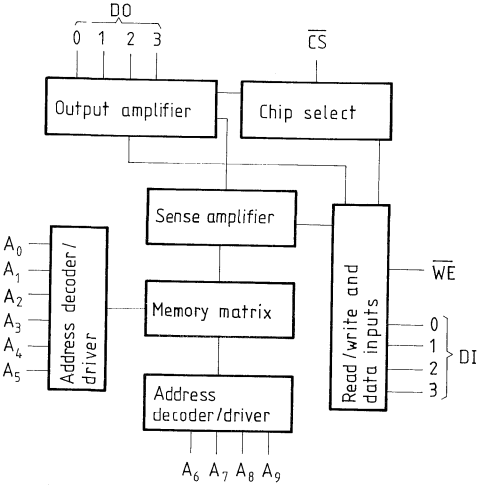
Pin configuration (top view)



Pin names

A_0–A_5	Address inputs
DI_0–DI_3	Data inputs
DO_0–DO_3	Data outputs
$\overline{CS}$	Chip select input
$\overline{WE}$	Read/write input
V_{CC}, V_{CCO}	GND 1, GND 2
V_{EE}	Supply voltage
NC	Not connected

Block diagram



Absolute maximum ratings[1])

Supply voltage	V_{EE}	–4.05 to –4.95	V
Input voltage	V_I	GND to V_{EE}	
Output current	I_O	–50	mA
Ambient temperature	T_{amb}	0 to 85	°C
Storage temperature	T_s	–55 to 125	°C

Functional description

Four of the 4096 cells of the memory matrix are selected with the 10 address bits A_0 to A_9 via the X and Y decoders.

The four cells can be read or rewritten according to the state of the write/read control, which depends on the signal at the $\overline{WE}$ input.

During the read cycle, the information from the selected cells is moved via the output amplifier to the data output. The values available at the data input DI have no effect.

During the write cycle, the values available at DI are transferred to the four selected cells. In this state, the output amplifier is disabled and DO always has "Low" level.

The write/read control and the output amplifier can be disabled or enabled simultaneously via the chip select input $\overline{CS}$. If they are disabled, it is not possible to read data from or write data into the memory, regardless of the logical values at the remaining inputs. The contents of the memory remain unaffected.

[1]) Stresses above those listed under "Absolute maximum ratings" may cause permanent damage to the device. Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is, therefore, advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

The device is a non-inverting memory, i. e. the logical value written in at DI is identical with the logical value read out at DO. In all operating states, a "Low" level is present at the output, except when a "High" level is read. This characteristic makes it possible to connect the outputs of several devices together, the common output then having "High" level only when a selected chip generates a "High" level.

This type of connection (OR-tied connection) makes it possible to assemble memories with virtually unlimited capacities.

Truth table

Input $\overline{CS}$	$\overline{WE}$	DI	Output Open emitter	Operating mode
H	X	X	L	Disabled
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	H/L	Read "1"/"0"

Operating and test conditions

$T_{amb} = 25°C$, $V_{CC} = 0\,V$, $V_{EE} = -4.5\,V \pm 10\%$, output load $50\,\Omega$ to $-2\,V$

DC characteristics ($T_{amb} = 25°C$)

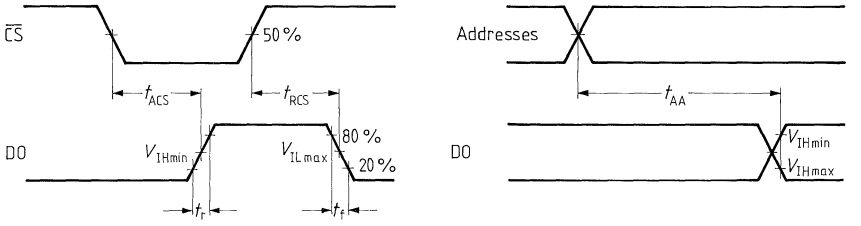
		Test conditions	Min.	Typ.	Max.	Unit
Supply current	I_{EE}			200		mA
H-output voltage	V_{QH}	$V_I = V_{IH\,max}$	−1025	−955	−880	mV
L-output voltage	V_{QL}	or $V_{IL\,min}$	−1810	−1705	−1620	mV
H-output voltage	V_{QHC}	$V_I = V_{IH\,min}$	−1035			mV
L-output voltage	V_{QLC}	or $V_{IL\,max}$			−1610	mV
H-input voltage	V_{IH}		−1215		−880	mV
L-input voltage	V_{IL}		−1810		−1425	mV
H-input current (A_0–A_9)	I_{IH}	$V_I = V_{IH\,max}$		10		µA
H-input current ($\overline{CS}$, DI, $\overline{WE}$)	I_{IH}	$V_I = V_{IH\,max}$		20		µA
L-input current (A_0–A_5)	I_{IL}	$V_I = V_{IL\,max}$		10		µA
L-input current (A_6–A_9, $\overline{WE}$, $\overline{CS}$, DI)	I_{IL}	$V_I = V_{IL\,max}$		0		µA
Power dissipation	P_{tot}			0.9		W

Operating and test conditions

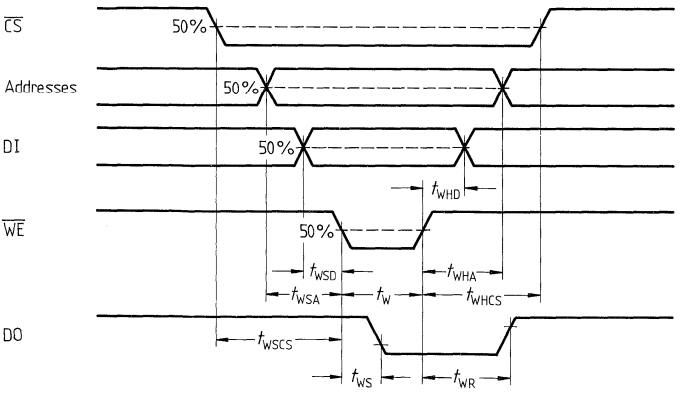
$T_{amb} = 0$ to 85° C, $V_{CC} = 0$ V, $V_{EE} = -4.5$ V ± 10 %

AC conditions

Read cycle		Min.	Typ.	Max.	Unit
Chip select access time	t_{ACS}		12	15	ns
Chip select recovery time	t_{RCS}		12	15	ns
Address access time	t_{AA}		20	25	ns
Rise time	t_r	0.5	0.7	0.9	ns
Fall time	t_f	0.5	0.7	0.9	ns



Write cycle		Min.	Typ.	Max.	Unit
Write pulse width	t_W	25	20		ns
Data set-up time	t_{WSD}	5	0		ns
Data hold time	t_{WHD}	5	3		ns
Address set-up time	t_{WSA}	8	5		ns
Address hold time	t_{WHA}	5	3		ns
Chip select set-up time	t_{WSCS}	5	0		ns
Chip select hold time	t_{WHCS}	5	0		ns
Write disable time	t_{WS}	10	7		ns
Write recovery time	t_{WR}	10	7		ns



Preliminary data

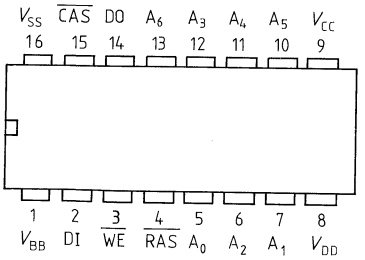
Type	Ordering code	Package outline
HYB 4116-A 3	Q67100–Q186	Ceramic / Figure No. 2
HYB 4116-A 4	Q67100–Q187	Ceramic / Figure No. 2
HYB 4116-P 3	Q67100–Q219	Plastic / Figure No. 3
HYB 4116-P 4	Q67100–Q220	Plastic / Figure No. 3

The HYB 4116 is a dynamic random access memory fabricated in n-channel silicon gate technology, using double layer polysilicon.

The dynamic one-transistor cell ensures high packing density and high speed. Moreover, multiplexing of the address signals permits the use of the space-saving 16-pin dual in-line package.

- N-channel double silicon gate technology
- 16,384 x 1 bit organization, fully decoded
- Separate data input and output
- All inputs including clocks TTL compatible
- Low power dissipation: 462 mW active, 20 mW standby
- On-chip latches for address and data in
- 200 ns access time, 375 ns cycle time (HYB 4116-A 3; P 3)
- 250 ns access time, 410 ns cycle time (HYB 4116-A 4; P 4)
- Three-state output, 2 TTL load
- Compatible with MK 4116
- 128 refresh cycles
- Input for chip select
- Data output unlatched
- ± 10% tolerance for all power supplies

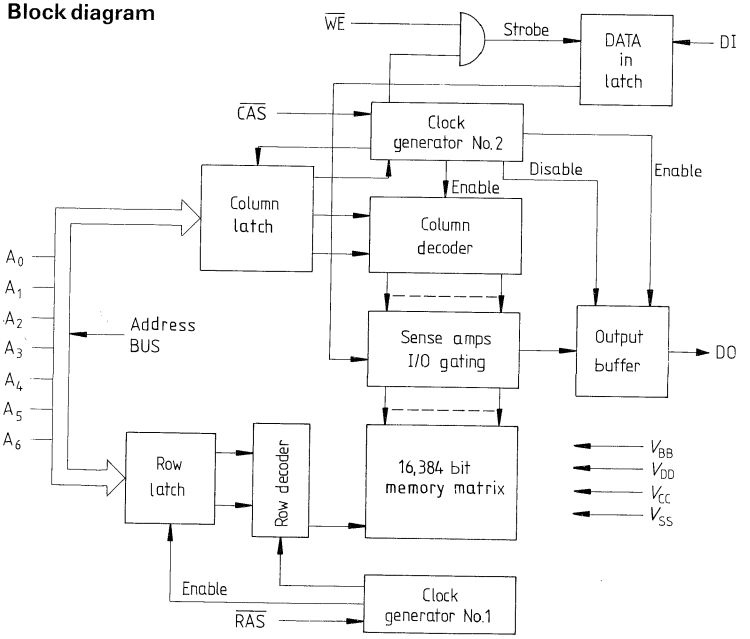
Pin configuration (top view)



Pin names

A_0–A_6	Address inputs
$\overline{CAS}$	Column address strobe
DI	Data input
DO	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Read/write clock
V_{BB}	−5 V
V_{CC}	+5 V
V_{DD}	+12 V
V_{SS}	0 V (Ground)

Block diagram



Functional description

Addressing ($A_0 - A_6$)

For selecting one of the 16,384 memory cells, a total of 14 address bits is required which is consecutively applied via pins A_0 to A_6 by means of two strobes (address multiplexing). First, the seven row addresses are called up and accepted with strobe $\overline{RAS}$ into the row select buffer. Following this, the seven column addresses are deposited in the column select buffer with $\overline{CAS}$. It should be noted that the address signals are available in their steady-state condition at the time of the negative pulse edge of $\overline{RAS}$ and $\overline{CAS}$, respectively.

$\overline{RAS}$ and $\overline{CAS}$ determine the starting point of the internal clock control.
$\overline{RAS}$ initiates row decoding and activates the read amplifier.
$\overline{CAS}$ controls column decoding as well as the data input and output amplifiers.

Read/write ($\overline{WE}$)

Read and write operations are executed when the write enable signal $\overline{WE}$ is at "H" or "L". Data input D is disabled as long as reading takes place.

The shortest write cycle time is obtained when $\overline{WE}$ goes to logic "L" ahead of or simultaneously with $\overline{CAS}$ ("early write"). The write data is then accepted into the input data memory by means of $\overline{CAS}$.

Delayed writing, read/modify/write

If writing or read/modify/write is delayed, $\overline{CAS}$ is already at logic "L" so that the write data is transferred to the input data memory with the subsequent $\overline{WE}$ signal.

Data input (DI)

Data can be put in during a write or a read/modify/write cycle.The strobe for the data input is the later of the signals $\overline{WE}$ or $\overline{CAS}$ to make its negative transition.

Data output (DO)

The data output has three state capability (Tri-state logic) and is designed for driving two TTL loads. Compared to the input data the output data is not inverted. In a read cycle, the read data is available after access time t_{CAC} referred to $\overline{CAS}$. At the end of the read cycle, when $\overline{CAS}$ is again "H", the data output assumes again the high impedance state.

During read/modify/write the data output contains the data read from the selected cell as in the read cycle. For "early write" the output pin is in the high impedance state throughout the entire cycle.

Refresh cycle

To maintain data in the dynamic memory cells, each row address must be called up at least every two milliseconds. A total of 128 refresh cycles must be executed for all row addresses during this 2 millisecond period.

During writing or reading the data in the 128 memory cells of a row-line is automatically refreshed.

Power on

After power is applied to the device, the HYB 4116 requires several cycles before proper device operation is ensured. Any 8 cycles which perform refresh are adequate to this purpose.

Absolute maximum ratings[1])

Voltage on any pin relative to V_{BB}		–0.5 to 20	V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS}		–1 to 15	V
$V_{BB} - V_{SS}$ ($V_{DD} - V_{SS} \geqq 0$ V)		0	V
Operating temperature range	T_{amb}	0 to 70	°C
Storage temperature range	T_s	–65 to 150	°C
Power dissipation	P_{tot}	1	W
Standby power dissipation		20	mW

Operating and test conditions

$T_{amb} = 0$ to $+70$° C, $V_{SS} = 0$ V, $V_{DD} = +12$ V ± 10%, $V_{BB} = -5$ V ± 10%, $V_{CC} = +5$ V ± 10%

DC characteristics[2])

		Test conditions	Min.	Typ.	Max.	Unit
H-input voltage, (all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)[3])	V_{IH}		2.4		7	V
H-input voltage ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)[3])	V_{IHC}		2.7		7	V
L-input voltage[3])	V_{IL}		–1		0.8	V
H-output voltage	V_{OH}	$I_O = -5$ mA	2.4		V_{CC}	V
L-output voltage	V_{OL}	$I_O = 4.2$ mA			0.4	V
V_{DD} supply current[4])	I_{DD1}				35	mA
V_{DD} standby current	I_{DD2}	$\overline{RAS}$ at V_{IH}, $\overline{CAS}$ at V_{IH}			1.5	mA
Average V_{DD} current during refresh[4])	I_{DD3}	$\overline{RAS}$ cycling, $\overline{CAS}$ at V_{IH}			27	mA

[1]) Stresses above those listed unter "Absolute maximum ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.

[2]) The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC} and V_{SS} should never be 0.3 V, or more negative than V_{BB}.

[3]) Over and undershooting on input levels of 6.5 V or –2 V for a period of 30 ns will not influence function and reliability of the device.

[4]) I_{DD} depends on frequency of operation. Maximum current is measured at the fastest cycle rate.

Operating and test conditions

T_{amb} = 0 to +70° C, V_{SS} = 0 V, V_{DD} = +12 V ± 10%, V_{BB} = –5 V ± 10%, V_{CC} = +5 V ± 10%

DC characteristics[1])

		Test conditions	Min.	Typ.	Max.	Unit
Input leakage current[3])	$I_{I(L)}$		–10		10	µA
Output leakage current	$I_{O(L)}$	$\overline{CAS}$ at V_{IH}, V_O = V_{SS} to V_{CC}	–10		10	µA
V_{CC} standby current[2])	I_{CC}	$\overline{CAS}$ at V_{IH}, $\overline{RAS}$ at V_{IH}	–10		10	µA
Average V_{BB} supply current	I_{BB1}				200	µA
V_{BB} standby current	I_{BB2}				100	µA

Capacitances

Input capacitance[4]) (A_0–A_6), DI	C_{I1}				5	pF
Input capacitance[4]) $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}				10	pF
Output capacitance[4])	C_O	DO = Three state			7	pF

[1]) The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, V_{SS} should never be 0.3 V more negative than V_{BB}.

[2]) V_{CC} is connected to output buffer only.

[3]) All device pins at 0 V except V_{BB} at –5 V and pin under test which is at +7 V.

[4]) Effective capacitance calculated from the equation $C = \frac{I \cdot \Delta t}{\Delta V}$ with ΔV = 3 V.

Operating and test conditions

$T_{amb} = 0$ to $+70°C$, $V_{SS} = 0V$, $V_{DD} = +12V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{CC} = +5V \pm 10\%$

AC characteristics[1])

		HYB 4116 -A3/-P3		HYB 4116 -A4/-P4		Unit
		Min.	Max.	Min.	Max.	
Random read or write cycle time[2])	t_{RC}	375		410		ns
Read/write cycle time[2])	t_{RWC}	375		465		ns
Read/modify/write cycle time[2])	t_{RMWC}	415		515		ns
Access time from $\overline{RAS}$[3])[4])	t_{RAC}		200		250	ns
Access time from $\overline{CAS}$[3])[5])	t_{CAC}		135		165	ns
Output buffer turn-off delay[6])	t_{OFF}	0	50	0	60	ns
$\overline{RAS}$ precharge time	t_{RP}	120		150		ns
$\overline{RAS}$ pulse width	t_{RAS}	200	10^4	250	10^4	ns
$\overline{RAS}$ hold time	t_{RSH}	135		165		ns
$\overline{CAS}$ hold time	t_{CSH}	200		250		ns
$\overline{CAS}$ pulse width	t_{CAS}	135	10^4	165	10^4	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time[7])	t_{RCD}	25	65	35	85	ns
Row address set-up time	t_{ASR}	0		0		ns
Row address hold time	t_{RAH}	25		35		ns
Column address set-up time	t_{ASC}	–10		–10		ns
Column address hold time	t_{CAH}	55		75		ns
Column address hold time referred to $\overline{RAS}$	t_{AR}	120		160		ns
Transition time (rise and fall)	t_T	3	50	3	50	ns
Read command set-up time (RMW)	t_{RCS}	0		0		ns
Read command hold time	t_{RCH}	0		0		ns
Write command hold time	t_{WCH}	55		75		ns
Write command hold time referred to $\overline{RAS}$	t_{WCR}	120		160		ns
Write command set-up time[8])	t_{WCS}	–20		–20		ns

For notes see next page

AC characteristics[1])

		HYB 4116 -A3/-P3 Min.	HYB 4116 -A3/-P3 Max.	HYB 4116 -A4/-P4 Min.	HYB 4116 -A4/-P4 Max.	Unit
Write command pulse width	t_{WP}	55		75		ns
Writte command to $\overline{RAS}$ lead time	t_{RWL}	80		100		ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	80		100		ns
Data in set-up time	t_{DS}	0		0		ns
Data in hold time[9])	t_{DH}	55		75		ns
Data in hold time[9]) referred to $\overline{RAS}$	t_{DHR}	120		160		ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	–20		–20		ns
Refresh period	t_{RF}		2		2	ms
$\overline{CAS}$ to $\overline{WE}$ delay[8])	t_{CWD}	95		115		ns
$\overline{RAS}$ to $\overline{WE}$ delay[8])	t_{RWD}	160		200		ns

Notes

[1]) $V_{IHC\,(min)}$ or $V_{IH\,(min)}$ and $V_{IL\,(min)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

[2]) The specifications for $t_{RC\,(min)}$, $t_{RWC\,(min)}$ and t_{RMWC} are only used to indicate the cycle time at which proper operation over full temperature range ($0°C \leqq T_A \leqq 70°C$) is assured.

[3]) Measured with a load equivalent to two TTL loads and 100 pF.

[4]) Assumes that $t_{RCD} \leqq t_{RCD\,(max)}$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

[5]) Assumes that $t_{RCD} \geqq t_{RCD\,(max)}$.

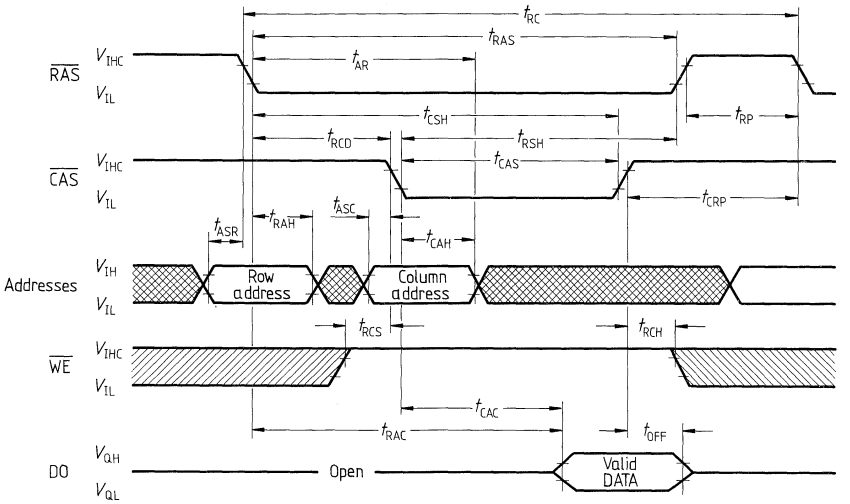
[6]) $t_{OFF\,(max)}$ defines the time at which the output achieves the open circuit condition and is not referred to output voltage levels.

[7]) Operation within the $t_{RCD\,(max)}$ limit ensures that $t_{RAC\,(max)}$ can be met. $t_{RCD\,(max)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD\,(max)}$ limit, then access time is controlled exclusively by t_{CAC}.

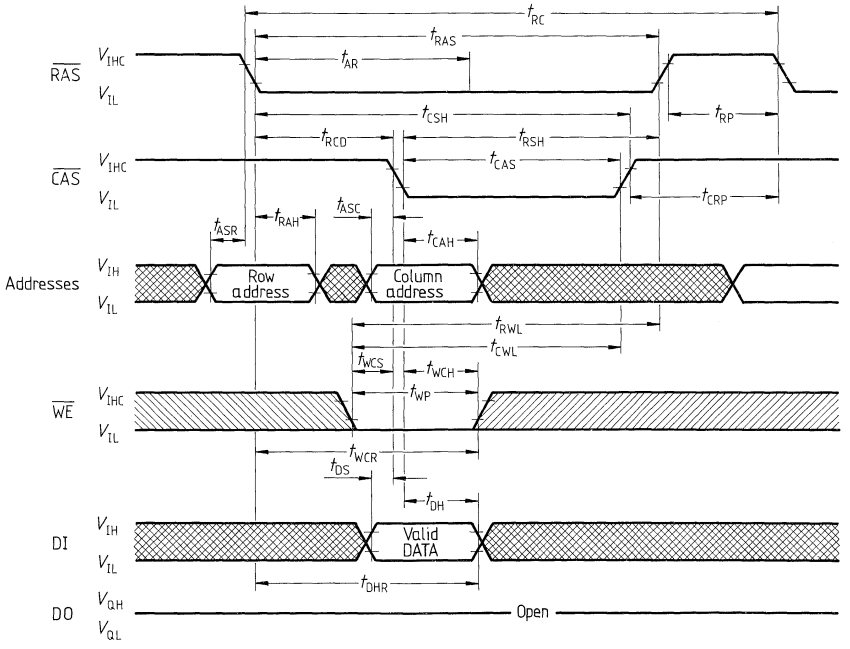
[8]) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geqq t_{WCS\,(min)}$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD\,(min)}$ and $t_{RWD} \leqq t_{RWD\,(min)}$, the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

[9]) t_{DS} and t_{DH} are referred to the leading edge of $\overline{CAS}$ in early write cycles, and to the leading edge of $\overline{WE}$ in delayed write or read-modify-write cycles.

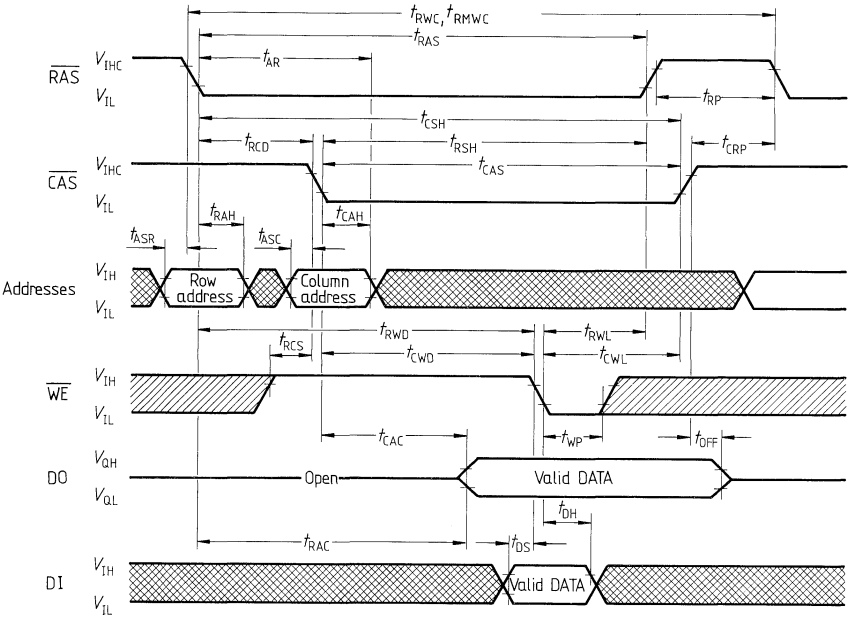
Read cycle



Write cycle (Early write)



Read-write/Read-modify-write cycle



Preliminary data

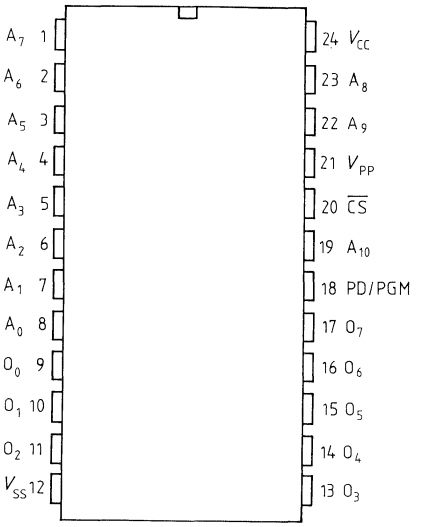
Type	Ordering code	Package outline
SAB 2716	Q67120–R44	Figure No. 5

UV erasable and electrically programmable ROM. "Floating gate" technology.

Features

- 2K × 8 bit organization
- Data retention 10 years min. at 70° C, powered or unpowered
- Unlimited number of read cycles
- Unlimited number of program-erase cycles
- Global erasure with UV light
- TTL pulse controlled programming
- Single address location programming
- Pin compatible with 16K ROMs 2316 E, SAB 8316, AM 9218
- Completely static operation
- Inputs and outputs TTL compatible
- Three-state outputs
- Low power dissipation, 535 mW max. active power / 132 mW standby power
- Fast access time, 450 ns max.

Pin configuration (top view)



Pin names

A_0–A_{10}	Address inputs
O_0–O_7	Data inputs/outputs
$\overline{CS}$	Chip select
V_{PP}	Program supply voltage
V_{CC}	Power supply
PD/PGM	Power down/program
V_{SS}	0 V (GND)

The Siemens SAB 2716 is a nonvolatile ultraviolet erasable and electrically programmable read only memory (EPROM) organized as 2048 × 8 bits. It operates from a single 5 V power supply and has a static standby mode. The total programming time for all 16,384 bits is only 100 seconds.

Three modes of operation are selectable:

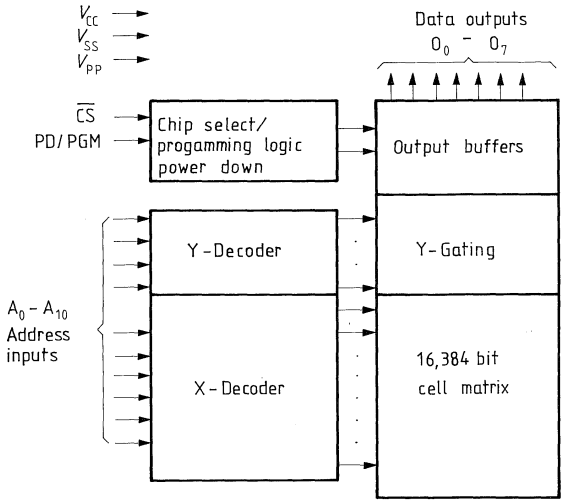
Read: with V_{PP} at 5 V

Program: with V_{PP} at 25 V
Programming an 8 bit word is achieved by activating PD/PGM for 50 ms.
Address sequence as required.

Standby: with $V_{PP} = 5$ V and PD/PGM = V_{IH}

The memory is manufactured in n-channel, double polysilicon and floating gate technology.

Block diagram



Absolute maximum ratings[1])

V_{CC} supply voltage	V_{CC}	7 to −0.3	V
V_{PP} supply voltage	V_{PP}	27 to −0.3	V
Input or output voltages	V_I	−0.3 to 7	V
Temperature under bias	T_{amb}	0 to 70	°C
Storage temperature	T_s	−55 to 125	°C

Mode selection

$V_{SS} = 0\,V$ (Ground), $V_{CC} = +5\,V$

Mode \ Pin		PD/PGM (18)	$\overline{CS}$ (20)	V_{PP}, V (21)	Data inputs/outputs (9–11, 13–17)
Read	selected	V_{IL}	V_{IL}	+5	Data out
	deselected	don't care	V_{IH}	+5	High Z
Standby		V_{IH}	don't care	+5	High Z
Program	selected	$V_{IL} \rightarrow V_{IH} \rightarrow V_{IL}$ one pulse	V_{IH}	+25	Data in
	inhibit	V_{IL}	V_{IH}	+25	High Z
	verify	V_{IL}	V_{IL}	+25	Data out

[1]) Stresses above those listed unter "Absolute maximum ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Read operation

$V_{SS} = 0\,V$ (Ground), $V_{CC} = +5\,V \pm 5\%$[1]), $V_{PP} = V_{CC} \pm 0.6\,V$[5]), $T_{amb} = 0°C$ to $70°C$

DC and operating characteristics

		Test conditions	Min.	Typ.	Max.	Unit
Input load current	I_{LI}	$V_I = 5.25\,V$			10	µA
Output leakage current	I_{LO}	$V_O = 5.25\,V$			10	µA
V_{PP} supply current	I_{PP1}	$V_{PP} = 5.85\,V$			7	mA
V_{CC} supply current (standby)	I_{CC1}	PD/PGM = V_{IH}; $\overline{CS} = V_{IL}$		10	25	mA
V_{CC} supply current (active)	I_{CC2}	$\overline{CS}$ = PD/PGM = V_{IL}		57	100	mA
L-input voltage	V_{IL}		−0.1		0.8	V
H-input voltage	V_{IH}		2.2		$V_{CC}+1$	V
L-output voltage	V_{OL}	$I_{OL} = 2.1\,mA$			0.45	V
H-output voltage	V_{OH}	$I_{OH} = 0.4\,mA$	2.4			V

AC characteristics

Address to output delay	t_{ACC1}	PD/PGM = V_{IL}; $\overline{CS} = V_{IL}$		250	450	ns
PD/PGM to output delay	t_{ACC2}			280	450	ns
$\overline{CS}$ to output delay (output active)	t_{CO}	PD/PGM = V_{IL}			120	ns
PD/PGM to output float	t_{PF}		0		100	ns
Chip deselect to output float	t_{DF}	PD/PGM = V_{IL}	0		100	ns
Address to output hold	t_{OH}	PD/PGM = $\overline{CS} = V_{IL}$	0			ns

For notes see page 364

AC test conditions

Output load: 1 TTL gate and $C_L = 100\,pF$
Input rise and fall times (10% to 90%): $\leqq 20\,ns$
Input pulse levels: 0.8 and 2.2 V
Timing measurement reference level: Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

Programming operation

$V_{SS} = 0\,V$ (Ground), $V_{CC} = +5\,V \pm 5\%$[1]), $V_{PP} = +25\,V \pm 1\,V$[1])[3])[4]); $T_{amb} = 25°C \pm 5°C$

DC operating characteristics

		Test conditions	Min.	Typ.	Max.	Unit
Input load current	I_{LI}	$V_I = 5.25\,V/0.45\,V$			10	µA
V_{CC} supply current	I_{CC}				100	mA
V_{PP} supply current	I_{PP1}	PD/PGM = V_{IL}			7	mA
V_{PP} supply current during programming pulse	I_{PP2}	PD/PGM = V_{IH}			30	mA
L-input voltage	V_{IL}		−0.1		0.8	V
H-input voltage	V_{IH}		2.2		$V_{CC}+1$	V

AC characteristics

Address set-up time	t_{AS}		2			µs
Address hold time	t_{AH}		2			µs
Data set-up time	t_{DS}		2			µs
Data hold time	t_{DH}		2			µs
$\overline{CS}$ set-up time	t_{CSS}		2			µs
$\overline{CS}$ hold time	t_{CSH}		2			µs
Chip select to output float delay	t_{DF}		0		120	ns
Chip select to output delay	t_{CO}	PD/PGM = V_{IL}			120	ns
Program pulse width	t_{PW}		45		55	ms
Program pulse rise time	t_{PRT}		5			ns
Program pulse fall time	t_{PFT}		5			ns

For notes see page 364

AC test conditions

Output load: 1 TTL-gate and $C_L = 100\,pF$
Input rise and fall times (10% to 90%): ≦ 20 ns
Input pulse level: 0.8 V and 2.2 V
Timing measurement reference level: Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

Capacitances (T_{amb} = 25° C, f = 1 MHz)

		Test conditions	Min.	Typ.[2])	Max.	Unit
Input capacitance	C_I	V_I = 0 V		4	6	pF
Output capacitance	C_O	V_O = 0 V		8	12	pF

Notes:

[1]) V_{CC} must be applied simultaneously or before V_{PP} and be removed simultaneously or after V_{PP}.

[2]) Typical values are for T_{amb} = 25° C and nominal supply voltages.

[3]) Care must be taken when switching the V_{PP} supply voltage to prevent overshoot exceeding the maximum allowable voltages of + 26 V on the V_{PP} pin.

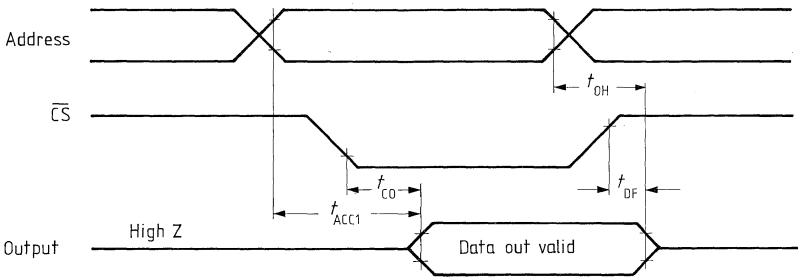
[4]) The SAB 2716 must not be inserted into or removed from a board with V_{PP} at 25 V ± 1 V to prevent damage from the device.

[5]) The tolerance of 0.6 V allows the use of a driver circuit for switching the V_{PP} supply pin from V_{CC} for reading to 25 V for programming.

[6]) $t_{ACC\,2}$ is referenced to PD/PGM or the address whichever occurs last.

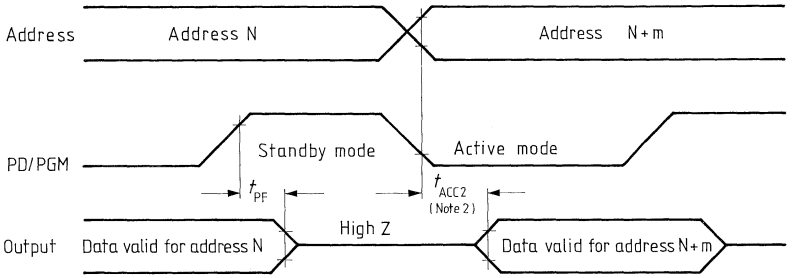
Read mode

PD/PGM = V_{IL}



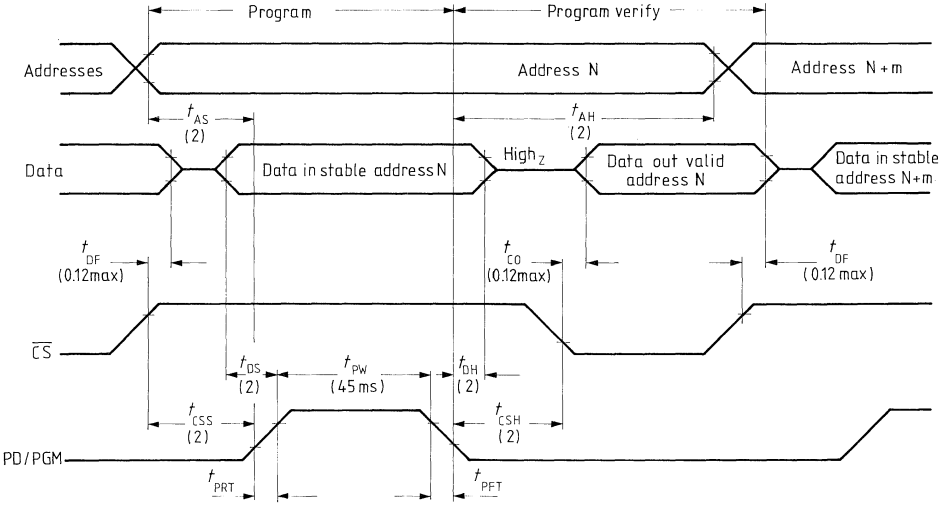
Standby mode

$\overline{CS}$ = V_{IL}



Program mode

$V_{PP} = 25\,V \pm 1\,V$



Note

All times shown in parentheses are minimum times and are µs unless otherwise noted.

Device operation

The power supply $V_{CC} = +5$ V remains unchanged for all 6 modes. The power supply $V_{PP} = +25$ V during the 3 program modes and in the other modes is +5 V. All other inputs have TTL level for all 6 modes.

Read mode

With PD/PGM = V_{IL} the device is in read mode and works as an ROM. The $\overline{CS}$ pin serves to gate data to the data outputs that otherwise are in high impedance. The outputs of two or more devices may be or-tied. To prevent data bus contention only one device at a line should have its outputs enabled by $\overline{CS}$.

Standby mode

With PD/PGM = V_{IH} the power dissipation reduces by 75%. The outputs are in high impedance.

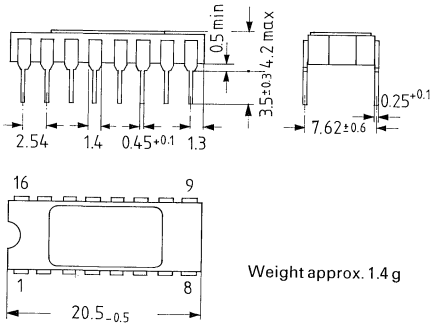
Programming mode

After each erasure all bits are in the logic "1" state. After programming a "0", the selected bit be in the logic "0" state, whatever the previous state was. By programming a logic "1" the logic state of the selected bit will not be changed, i.e. a "0" remains a "0", a "1" remains a "1". Changing a "0" to a "1" is accomplished only by block erasure with UV light. Thus, when an erasured device is programmed, exactly the programmed data will appear at the outputs when the device is read. With $V_{PP} = 25$ V and $\overline{CS} = V_{IH}$ the device is in program mode. The data outputs O_0 to O_7 are in high impedance. Programming an 8 bit word is accomplished by application of the desired addresses and data, followed by pulsing the PD/PGM input to the logic "1" level for 50 ms. To verify correct programming, it is possible to read the memory cells at the same address with $\overline{CS}$ and PD/PGM = V_{IH} and $V_{PP} = 25$ V. Any location may be programmed at any time, either individually, sequentially, or randomly.

Erase mode

The recommended erasure procedure for the SAB 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12 mW/cm² power rating. The SAB 2716 should be placed within 1 inch from the lamp tubes during erasure. After each erasure, all bits of the SAB 2716 are in the „1" state.

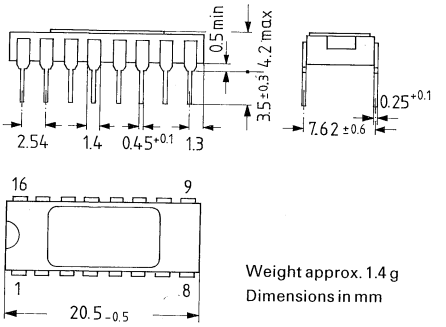
Ceramic package
16 pins



Weight approx. 1.4 g

Figure 1

Ceramic package
16 pins

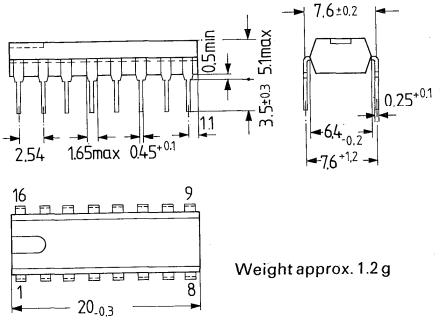


Weight approx. 1.4 g
Dimensions in mm

Figure 2

Plastic plug-in package 20 A 16 DIN 41866

16 pins

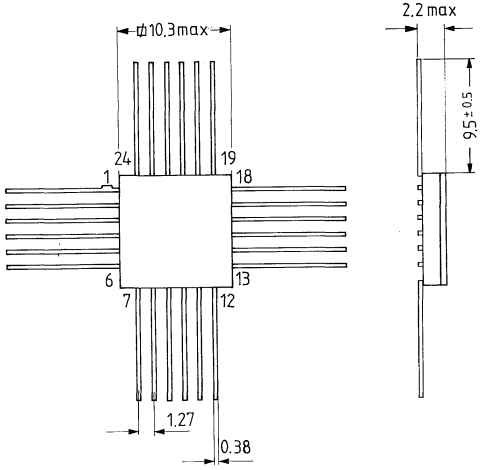


Weight approx. 1.2 g

Figure 3

Flat pack package

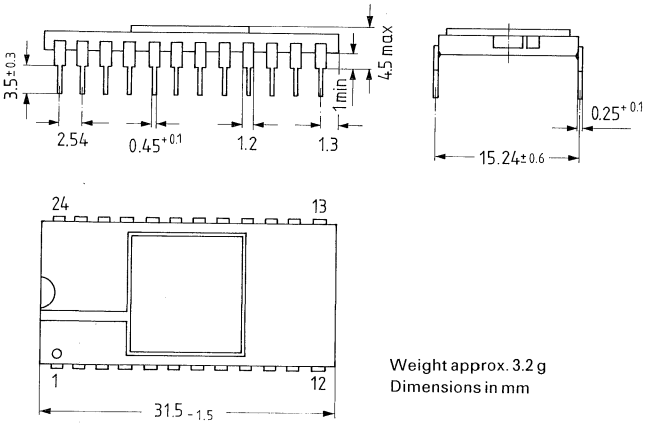
24 pins



Weight approx. 2.5 g
Dimensions in mm

Figure 4

Ceramic package with UV transparent window
24 pins



Weight approx. 3.2 g
Dimensions in mm

Figure 5

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